

80960JD

3.3 V EMBEDDED 32-BIT MICROPROCESSOR

• 3.3 V, 5 V Tolerant, Version of the 80960JD Processor

- Pin/Code Compatible with all 80960Jx Processors
- High-Performance Embedded Architecture
 - One Instruction/Clock Execution
 - Core Clock Rate is 2x the Bus Clock
 - Load/Store Programming Model
 - Sixteen 32-Bit Global Registers
 - Sixteen 32-Bit Local Registers (8 sets)
 - Nine Addressing Modes
 - User/Supervisor Protection Model
- Two-Way Set Associative Instruction Cache
 - 80960JD - 4 Kbyte
 - Programmable Cache Locking Mechanism
- Direct Mapped Data Cache
 - 80960JD - 2 Kbyte
 - Write Through Operation
- On-Chip Stack Frame Cache
 - Seven Register Sets Can Be Saved
 - Automatic Allocation on Call/Return
 - 0-7 Frames Reserved for High-Priority Interrupts
- On-Chip Data RAM
 - 1 Kbyte Critical Variable Storage
 - Single-Cycle Access
- 3.3 V Supply Voltage
 - 5 V Tolerant Inputs
 - TTL Compatible Outputs
- High Bandwidth Burst Bus
 - 32-Bit Multiplexed Address/Data
 - Programmable Memory Configuration
 - Selectable 8-, 16-, 32-Bit Bus Widths
 - Supports Unaligned Accesses
 - Big or Little Endian Byte Ordering
- High-Speed Interrupt Controller
 - 31 Programmable Priorities
 - Eight Maskable Pins plus NMI
 - Up to 240 Vectors in Expanded Mode
- Two On-Chip Timers
 - Independent 32-Bit Counting
 - Clock Prescaling by 1, 2, 4 or 8
 - Internal Interrupt Sources
- Halt Mode for Low Power
- IEEE 1149.1 (JTAG) Boundary Scan Compatibility
- Packages
 - 132-Lead Pin Grid Array (PGA)
 - 132-Lead Plastic Quad Flat Pack (PQFP)

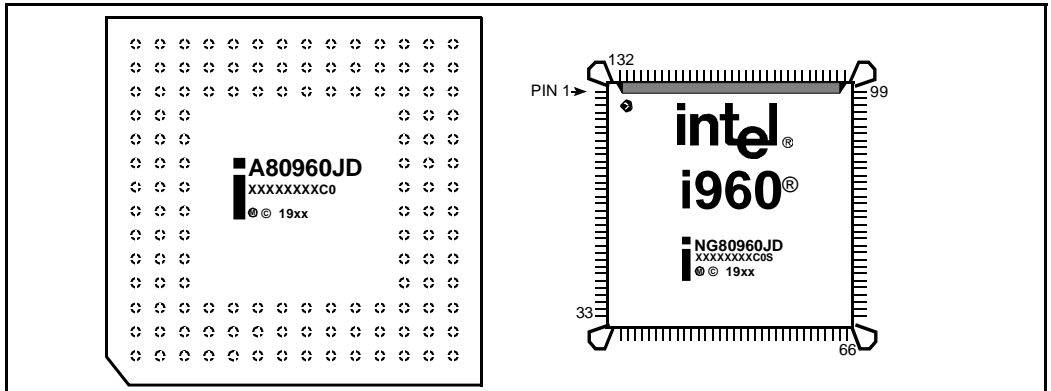


Figure 1. 80960JD Microprocessor

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80960JD

3.3 V EMBEDDED 32-BIT MICROPROCESSOR

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1.0 PURPOSE

This document contains preview information for the 80960JD microprocessor, including electrical characteristics and package pinout information. Detailed functional descriptions — other than parametric performance — are published in the *i960® Jx Microprocessor User's Guide (272483)*.

Throughout this data sheet, references to "80960Jx" indicate features which apply to all of the following:

- 80960JA — 5V, 2 Kbyte instruction cache, 1 Kbyte data cache
- 80L960JA — 3.3 V version of the 80960JA
- 80960JD — 5V, 4 Kbyte instruction cache, 2 Kbyte data cache and clock doubling
- 80960JD — 3.3V, 5V Tolerant version of the 80960JD
- 80960JF — 5V, 4 Kbyte instruction cache, 2 Kbyte data cache
- 80L960JF — 3.3 V version of the 80960JF

2.0 80960JD OVERVIEW

The 80960JD offers high performance to cost-sensitive 32-bit embedded applications. The 80960JD is object code compatible with the 80960 Core Architecture and is capable of sustained execution at the rate of one instruction per clock. This processor's features include generous instruction cache, data cache and data RAM. It also boasts a fast interrupt mechanism, dual programmable timer units and new instructions.

The 80960JD's clock doubler operates the processor core at twice the bus clock rate to improve execution performance without increasing the complexity of board designs.

Memory subsystems for cost-sensitive embedded applications often impose substantial wait state penalties. The 80960JD integrates considerable storage resources on-chip to decouple CPU execution from the external bus.

The 80960JD rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

A 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960JD to external components. The user programs physical and logical memory attributes through memory-mapped control registers

(MMRs) — an extension not found on the i960 Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment. The processor supports a homogeneous byte ordering model.

This processor integrates two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers, an extension to the familiar 80960 architecture.

The timer unit (TU) offers two independent 32-bit timers for use as real-time system clocks and general-purpose system timing. These operate in either single-shot or auto-reload mode and can generate interrupts.

The interrupt controller unit (ICU) provides a flexible means for requesting interrupts. The ICU provides full programmability of up to 240 interrupt sources into 31 priority levels. The ICU takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. Clock doubling reduces interrupt latency by 40% compared to the 80960JA/JF. Local registers may be dedicated to high-priority interrupts to further reduce latency. Acting independently from the core, the ICU compares the priorities of posted interrupts with the current process priority, off-loading this task from the core. The ICU also supports the integrated timer interrupts.

The 80960JD features a Halt mode designed to support applications where low power consumption is critical. The **halt** instruction shuts down instruction execution, resulting in a power savings of up to 90 percent.

The 80960JD's testability features, including ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

The *Solutions960®* program features a wide variety of development tools which support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

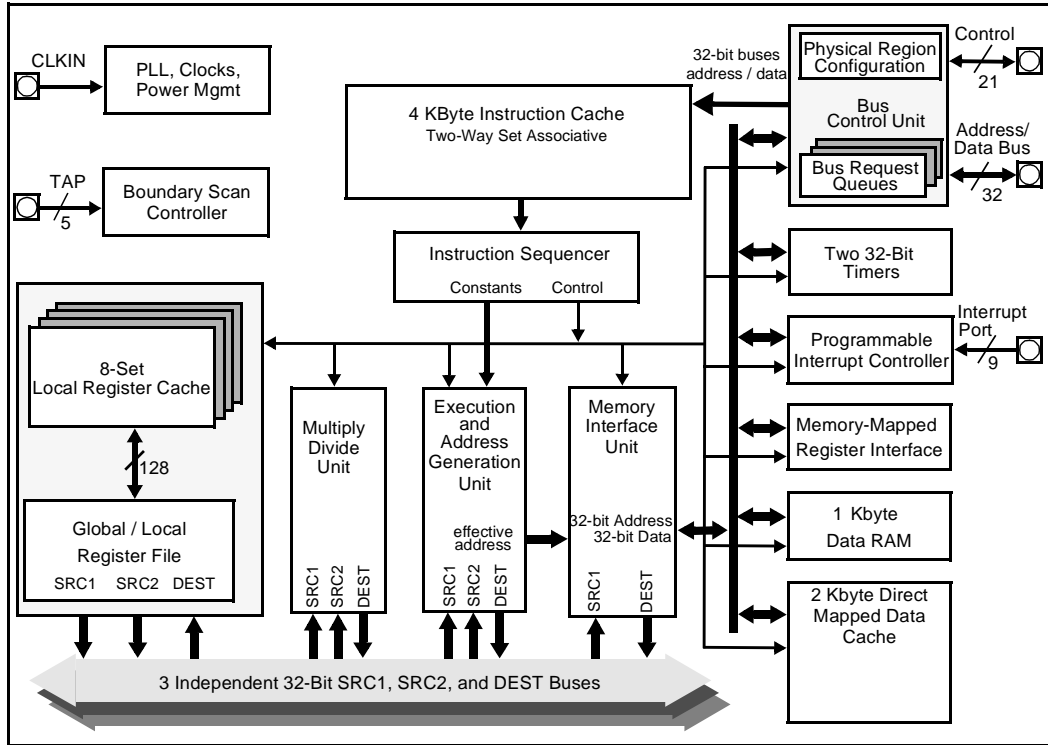


Figure 2. 80960JD Block Diagram

2.1 80960 Processor Core

The 80960Jx family is a scalar implementation of the 80960 Core Architecture. Intel designed this processor core as a very high performance device that is also cost-effective. Factors that contribute to the core's performance include:

- Core operates at twice the bus speed (80960JD only)
- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboard allow overlapped instruction execution
- 128-bit register bus speeds local register caching
- 4 Kbyte two-way set associative, integrated instruction cache

- 2 Kbyte direct-mapped, integrated data cache
- 1 Kbyte integrated data RAM delivers zero wait state program data

2.2 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960JD to external memory and peripherals. The BCU fetches instructions and transfers data at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960JD's bus controller to match an application's fundamental memory organization. Physical bus width is register-programmed for up to eight regions. Byte ordering and data caching are programmed through a group of logical memory templates and a defaults register.

The BCU's features include:

- Multiplexed external bus to minimize pin count
- 32-, 16- and 8-bit bus widths to simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Support for big or little endian byte ordering to facilitate the porting of existing program code
- Unaligned bus accesses performed transparently
- Three-deep load/store queue to decouple the bus from the core

Upon reset, the 80960JD conducts an internal self test. Then, before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the initialization boot record (IBR).

The user may examine the contents of the caches at any time by executing special cache control instructions.

2.3 Timer Unit

The timer unit (TU) contains two independent 32-bit timers which are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the TU registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960JD's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected. Clock prescaling is supported.

2.4 Priority Interrupt Controller

A programmable interrupt controller manages up to 240 external sources through an 8-bit external interrupt port. Alternatively, the interrupt inputs may be configured for individual edge- or level-triggered inputs. The interrupt unit (IU) also accepts interrupts from the two on-chip timer channels and a single Non-Maskable Interrupt (NMI) pin. Interrupts are serviced according to their priority levels relative to the current process priority.

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960JD exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space
- Interrupt microcode executes at twice the bus frequency

2.5 Instruction Set Summary

The 80960Jx adds several new instructions to the i960 core architecture. The new instructions are:

- Conditional Move
- Conditional Add
- Conditional Subtract
- Byte Swap
- Halt
- Cache Control
- Interrupt Control

Table 1 identifies the instructions that the 80960Jx supports. Refer to *i960® Jx Microprocessor User's Guide (272483)* for a detailed description of each instruction.

2.6 Faults and Debugging

The 80960Jx employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. In software, the 80960Jx may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.

2.7 Low Power Operation

Intel fabricates the 80960Jx using an advanced sub-micron manufacturing process. The processor's sub-micron topology provides the circuit density for optimal cache size and high operating speeds while

dissipating modest power. The processor also uses dynamic power management to turn off clocks to unused circuits.

Users may program the 80960Jx to enter Halt mode for maximum power savings. In Halt mode, the processor core stops completely while the integrated peripherals continue to function, reducing overall power requirements up to 90 percent. Processor execution resumes from internally or externally generated interrupts.

2.8 Test Features

The 80960Jx incorporates numerous features which enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960Jx provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960JD to electrically "remove" itself from a circuit board. This allows for system-level testing where a remote tester — such as an in-circuit emulator — can exercise the processor system.

The provided test logic does not interfere with component or circuit board behavior and ensures that components function correctly, connections between various components are correct, and various components interact correctly on the printed circuit board.

The JTAG Boundary Scan feature is an attractive alternative to conventional "bed-of-nails" testing. It can examine connections which might otherwise be inaccessible to a test system.

2.9 Memory-Mapped Control Registers

The 80960JD, though compliant with i960 series processor core, has the added advantage of memory-mapped, internal control registers not found on the i960 Kx, Sx or Cx processors. These give software the interface to easily read and modify internal control registers.

Each of these registers is accessed as a memory-mapped, 32-bit register. Access is accomplished through regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.10 Data Types and Memory Addressing Modes

As with all i960 family processors, the 80960Jx instruction set supports several data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960Jx provides a full set of addressing modes for C and assembly programming:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement
- IP with displacement

Table 1. 80960Jx Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load Store Move *Conditional Select Load Address	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry *Conditional Add *Conditional Subtract Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal *Byte Swap
Comparison	Branch	Call/Return	Fault
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	Processor Management	Atomic	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls *Halt System Control *Cache Control *Interrupt Control	Atomic Add Atomic Modify	

NOTES: Asterisk (*) denotes new 80960Jx instructions unavailable on 80960CA/CF, 80960KA/KB and 80960SA/SB implementations.

3.0 PACKAGE INFORMATION

The 80960JD is offered with three speeds and two package types. The 132-pin Pin Grid Array (PGA) device is specified for operation at $V_{CC} = 3.3\text{ V} \pm 5\%$ over a case temperature range of 0° to 100°C :

- A80960JD-66 (66 MHz core, 33 MHz bus)
- A80960JD-50 (50 MHz core, 25 MHz bus)
- A80960JD-40 (40 MHz core, 20 MHz bus)

The 132-pin Plastic Quad Flatpack (PQFP) devices will be specified for operation at $V_{CC} = 3.3\text{ V} \pm 5\%$ over a case temperature range of 0° to 100°C :

- NG80960JD-66 (66 MHz core, 33 MHz bus)
- NG80960JD-50 (50 MHz core, 25 MHz bus)
- NG80960JD-40 (40 MHz core, 20 MHz bus)

For complete package specifications and information, refer to Intel's *Packaging Handbook* (240800).

3.1 Pin Descriptions

This section describes the pins for the 80960JD in the 132-pin ceramic Pin Grid Array (PGA) package and 132-lead Plastic Quad Flatpack Package (PQFP).

Section 3.1.1, Functional Pin Definitions describes pin function; **Section 3.1.2, 80960Jx 132-Lead PGA Pinout** and **Section 3.1.3, 80960Jx PQFP Pinout** define the signal and pin locations for the supported package types.

3.1.1 Functional Pin Definitions

Table 2 presents the legend for interpreting the pin descriptions which follow. Pins associated with the bus interface are described in Table 3. Pins associated with basic control and test functions are described in Table 4. Pins associated with the Interrupt Unit are described in Table 5.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input pin only.
O	Output pin only.
I/O	Pin can be either an input or output.
–	Pin must be connected as described.
S	Synchronous. Inputs must meet setup and hold times relative to CLKIN for proper operation. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to CLKIN. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the processor's $\overline{\text{RESET}}$ pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(X) is driven to unknown state R(H) is pulled up to V_{CC}
H (...)	While the processor is in the hold state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the processor is halted, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output

Table 3. Pin Description — External Bus Signals (Sheet 1 of 4)

NAME	TYPE	DESCRIPTION															
AD31:0	I/O S(L) R(X) H(Z) P(Q)	<p>ADDRESS / DATA BUS carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 31:2 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD31:24, AD23:16, AD15:8 and AD7:0. During write operations, unused pins are driven to determinate values.</p> <p>SIZE, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction.</p> <table border="0"> <tr> <td>AD1</td> <td>AD0</td> <td>Bus Transfers</td> </tr> <tr> <td>0</td> <td>0</td> <td>1 Transfer</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 Transfers</td> </tr> <tr> <td>1</td> <td>0</td> <td>3 Transfers</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 Transfers</td> </tr> </table> <p>When the processor enters Halt mode, if the previous bus operation was a:</p> <ul style="list-style-type: none"> • write — AD31:2 are driven with the last data value on the AD bus. • read — AD31:4 are driven with the last address value on the AD bus; AD3:2 are driven with the value of A3:2 from the last data cycle. <p>Typically, AD1:0 reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.</p>	AD1	AD0	Bus Transfers	0	0	1 Transfer	0	1	2 Transfers	1	0	3 Transfers	1	1	4 Transfers
AD1	AD0	Bus Transfers															
0	0	1 Transfer															
0	1	2 Transfers															
1	0	3 Transfers															
1	1	4 Transfers															
ALE	O R(0) H(Z) P(0)	<p>ADDRESS LATCH ENABLE indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).</p>															
$\bar{A}LE$	O R(1) H(Z) P(1)	<p>ADDRESS LATCH ENABLE indicates the transfer of a physical address. $\bar{A}LE$ is the inverted version of ALE. This signal gives the 80960JD a high degree of compatibility with existing 80960Kx systems.</p>															
$\bar{A}DS$	O R(1) H(Z) P(1)	<p>ADDRESS STROBE indicates a valid address and the start of a new bus access. The processor asserts $\bar{A}DS$ for the entire T_a cycle. External bus control logic typically samples $\bar{A}DS$ at the end of the cycle.</p>															
A3:2	O R(X) H(Z) P(Q)	<p>ADDRESS3:2 comprise a partial demultiplexed address bus.</p> <p><i>32-bit memory accesses:</i> the processor asserts address bits A3:2 during T_a. The partial word address increments with each assertion of RDYRCV during a burst.</p> <p><i>16-bit memory accesses:</i> the processor asserts address bits A3:1 during T_a with A1 driven on the $\bar{BE}1$ pin. The partial short word address increments with each assertion of RDYRCV during a burst.</p> <p><i>8-bit memory accesses:</i> the processor asserts address bits A3:0 during T_a, with A1:0 driven on $\bar{BE}1:0$. The partial byte address increments with each assertion of RDYRCV during a burst.</p>															

Table 3. Pin Description — External Bus Signals (Sheet 2 of 4)

NAME	TYPE	DESCRIPTION																				
BE3:0	<p>O R(1) H(Z) P(1)</p>	<p>BYTE ENABLES select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding is dependent on the bus width of the memory region accessed:</p> <p><i>32-bit bus:</i></p> <p>$\overline{\text{BE}}3$ enables data on AD31:24 $\overline{\text{BE}}2$ enables data on AD23:16 $\overline{\text{BE}}1$ enables data on AD15:8 $\overline{\text{BE}}0$ enables data on AD7:0</p> <p><i>16-bit bus:</i></p> <p>$\overline{\text{BE}}3$ becomes Byte High Enable (enables data on AD15:8) $\overline{\text{BE}}2$ is not used (state is high) $\overline{\text{BE}}1$ becomes Address Bit 1 (A1) $\overline{\text{BE}}0$ becomes Byte Low Enable (enables data on AD7:0)</p> <p><i>8-bit bus:</i></p> <p>$\overline{\text{BE}}3$ is not used (state is high) $\overline{\text{BE}}2$ is not used (state is high) $\overline{\text{BE}}1$ becomes Address Bit 1 (A1) $\overline{\text{BE}}0$ becomes Address Bit 0 (A0)</p> <p>The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst. They remain active through the last T_d cycle.</p> <p>For accesses to 8- and 16-bit memory, the processor asserts the address bits in conjunction with A3:2 described above.</p>																				
WIDTH/ HLTD1:0	<p>O R(0) H(Z) P(1)</p>	<p>WIDTH/HALTED signals denote the physical memory attributes for a bus transaction:</p> <table border="0"> <tr> <td></td> <td>WIDTH/HLTD1</td> <td>WIDTH/HLTD0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td></td> <td>8 Bits Wide</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> <td>16 Bits Wide</td> </tr> <tr> <td>1</td> <td>0</td> <td></td> <td>32 Bits Wide</td> </tr> <tr> <td>1</td> <td>1</td> <td></td> <td>Processor Halted</td> </tr> </table> <p>The processor floats the WIDTH/HLTD pins whenever it relinquishes the bus in response to a HOLD request, regardless of prior operating state.</p>		WIDTH/HLTD1	WIDTH/HLTD0		0	0		8 Bits Wide	0	1		16 Bits Wide	1	0		32 Bits Wide	1	1		Processor Halted
	WIDTH/HLTD1	WIDTH/HLTD0																				
0	0		8 Bits Wide																			
0	1		16 Bits Wide																			
1	0		32 Bits Wide																			
1	1		Processor Halted																			
D/C	<p>O R(X) H(Z) P(Q)</p>	<p>DATA/CODE indicates that a bus access is a data access (1) or an instruction access (0). D/C has the same timing as W/R.</p> <p>0 = instruction access 1 = data access</p>																				
W/R	<p>O R(0) H(Z) P(Q)</p>	<p>WRITE/READ specifies, during a T_a cycle, whether the operation is a write (1) or read (0). It is latched on-chip and remains valid during T_d cycles.</p> <p>0 = read 1 = write</p>																				
DT/R	<p>O R(0) H(Z) P(Q)</p>	<p>DATA TRANSMIT / RECEIVE indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. DT/R never changes state when $\overline{\text{DEN}}$ is asserted.</p> <p>0 = receive 1 = transmit</p>																				

Table 3. Pin Description — External Bus Signals (Sheet 3 of 4)

NAME	TYPE	DESCRIPTION
$\overline{\text{DEN}}$	O R(1) H(Z) P(1)	<p>DATA ENABLE indicates data transfer cycles during a bus access. $\overline{\text{DEN}}$ is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. $\overline{\text{DEN}}$ is used with $\text{DT}/\overline{\text{R}}$ to provide control for data transceivers connected to the data bus.</p> <p>0 = data cycle 1 = not data cycle</p>
$\overline{\text{BLAST}}$	O R(1) H(Z) P(1)	<p>BURST LAST indicates the last transfer in a bus access. $\overline{\text{BLAST}}$ is asserted in the last data transfer of burst and non-burst accesses. $\overline{\text{BLAST}}$ remains active as long as wait states are inserted via the $\overline{\text{RDYRCV}}$ pin. $\overline{\text{BLAST}}$ becomes inactive after the final data transfer in a bus cycle.</p> <p>0 = last data transfer 1 = not last data transfer</p>
$\overline{\text{RDYRCV}}$	I S(L)	<p>READY/RECOVER indicates that data on AD lines can be sampled or removed. If $\overline{\text{RDYRCV}}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w).</p> <p>0 = sample data 1 = don't sample data</p> <p>The $\overline{\text{RDYRCV}}$ pin has another function during the recovery (T_r) state. The processor continues to insert additional recovery states until it samples the pin HIGH. This function gives slow external devices more time to float their buffers before the processor begins to drive address again.</p> <p>0 = insert wait states 1 = recovery complete</p>
$\overline{\text{LOCK}}/\overline{\text{ONCE}}$	I/O S(L) R(H) H(Z) P(1)	<p>BUS LOCK indicates that an atomic read-modify-write operation is in progress. The $\overline{\text{LOCK}}$ output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while it is asserting $\overline{\text{LOCK}}$. This prevents external agents from accessing memory involved in semaphore operations.</p> <p>0 = Atomic read-modify-write in progress 1 = Atomic read-modify-write not in progress</p> <p>ONCE MODE: The processor samples the $\overline{\text{ONCE}}$ input during reset. If it is asserted LOW at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins. The pin has a weak internal pullup which is active during reset to ensure normal operation when the pin is left unconnected.</p> <p>0 = ONCE mode enabled 1 = ONCE mode not enabled</p>
$\overline{\text{HOLD}}$	I S(L)	<p>HOLD: A request from an external bus master to acquire the bus. When the processor receives $\overline{\text{HOLD}}$ and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines and enters the T_h state. When $\overline{\text{HOLD}}$ is deasserted, the processor deasserts HOLDA and enters either the T_i or T_a state, resuming control of the address/data and control lines.</p> <p>0 = no hold request 1 = hold request</p>

Table 3. Pin Description — External Bus Signals (Sheet 4 of 4)

NAME	TYPE	DESCRIPTION
HOLDA	O R(Q) H(1) P(Q)	HOLD ACKNOWLEDGE indicates to an external bus master that the processor has relinquished control of the bus. The processor can grant HOLD requests and enter the T_h state during reset and while halted as well as during regular operation. 0 = hold not acknowledged 1 = hold acknowledged
BSTAT	O R(0) H(Q) P(0)	BUS STATUS indicates that the processor may soon stall unless it has sufficient access to the bus; see <i>i960[®] Jx Microprocessor User's Guide (272483)</i> . Arbitration logic can examine this signal to determine when an external bus master should acquire/relinquish the bus. 0 = no potential stall 1 = potential stall

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLKIN	I	CLOCK INPUT provides the processor's fundamental time base; both the processor core and the external bus run at the CLKIN rate. All input and output timings are specified relative to a rising CLKIN edge.
RESET	I A(L)	RESET initializes the processor and clears its internal logic. During reset, the processor places the address/data bus and control output pins in their idle (inactive) states. During reset, the input pins are ignored with the exception of $\overline{LOCK/ONCE}$, STEST and HOLD. The \overline{RESET} pin has an internal synchronizer. To ensure predictable processor initialization during power up, \overline{RESET} must be asserted a minimum of 10,000 CLKIN cycles with V_{CC} and CLKIN stable. On a warm reset, \overline{RESET} should be asserted for a minimum of 15 cycles.
STEST	I S(L)	SELF TEST enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of reset. When STEST is asserted, the processor performs its internal self-test and the external bus confidence test. When STEST is deasserted, the processor performs only the external bus confidence test. 0 = self test disabled 1 = self test enabled
FAIL	O R(0) H(Q) P(1)	FAIL indicates a failure of the processor's built-in self-test performed during initialization. FAIL is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: <ul style="list-style-type: none"> When self-test passes, the processor deasserts \overline{FAIL} and begins operation from user code. When self-test fails, the processor asserts \overline{FAIL} and then stops executing. 0 = self test failed 1 = self test passed
TCK	I	TEST CLOCK is a CPU input which provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	I S(L)	TEST DATA INPUT is the serial input pin for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port.

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TDO	O R(Q) HQ) P(Q)	TEST DATA OUTPUT is the serial output pin for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. TDO does not float during ONCE mode.
TRST	I A(L)	TEST RESET asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). When using the Boundary Scan feature, connect a pulldown resistor between this pin and V _{SS} . If TAP is not used, this pin must be connected to V _{SS} ; however, no resistor is required. See Section 4.3, Connection Recommendations (pg. 22).
TMS	I S(L)	TEST MODE SELECT is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing.
V _{CC}	–	POWER pins intended for external connection to a V _{CC} board plane.
V _{CCPLL}	–	PLL POWER is a separate V _{CC} supply pin for the phase lock loop clock generator. It is intended for external connection to the V _{CC} board plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
V _{CC5}	–	5 V REFERENCE VOLTAGE input is the reference voltage for the 5 V-tolerant I/O buffers. This signal should be connected to +5 V for use with inputs which exceed 3.3 V. If all inputs are from 3.3 V components, this pin should be connected to 3.3 V.
V _{SS}	–	GROUND pins intended for external connection to a V _{SS} board plane.
NC	–	NO CONNECT pins. Do not make any system connections to these pins.

Table 5. Pin Description — Interrupt Unit Signals

NAME	TYPE	DESCRIPTION
XINT7:0	I A(E/L)	<p>EXTERNAL INTERRUPT pins are used to request interrupt service. The XINT7:0 pins can be configured in three modes:</p> <p>Dedicated Mode: Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low) or edge (falling) sensitive.</p> <p>Expanded Mode: All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode.</p> <p>Mixed Mode: The XINT7:5 pins act as dedicated sources and the XINT4:0 pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to 010₂ internally.</p> <p>Unused external interrupt pins should be connected to V_{CC}.</p>
NMI	I A(E)	<p>NON-MASKABLE INTERRUPT causes a non-maskable interrupt event to occur. NMI is the highest priority interrupt source and is falling edge-triggered. If NMI is unused, it should be connected to V_{CC}.</p>

3.1.2 80960Jx 132-Lead PGA Pinout

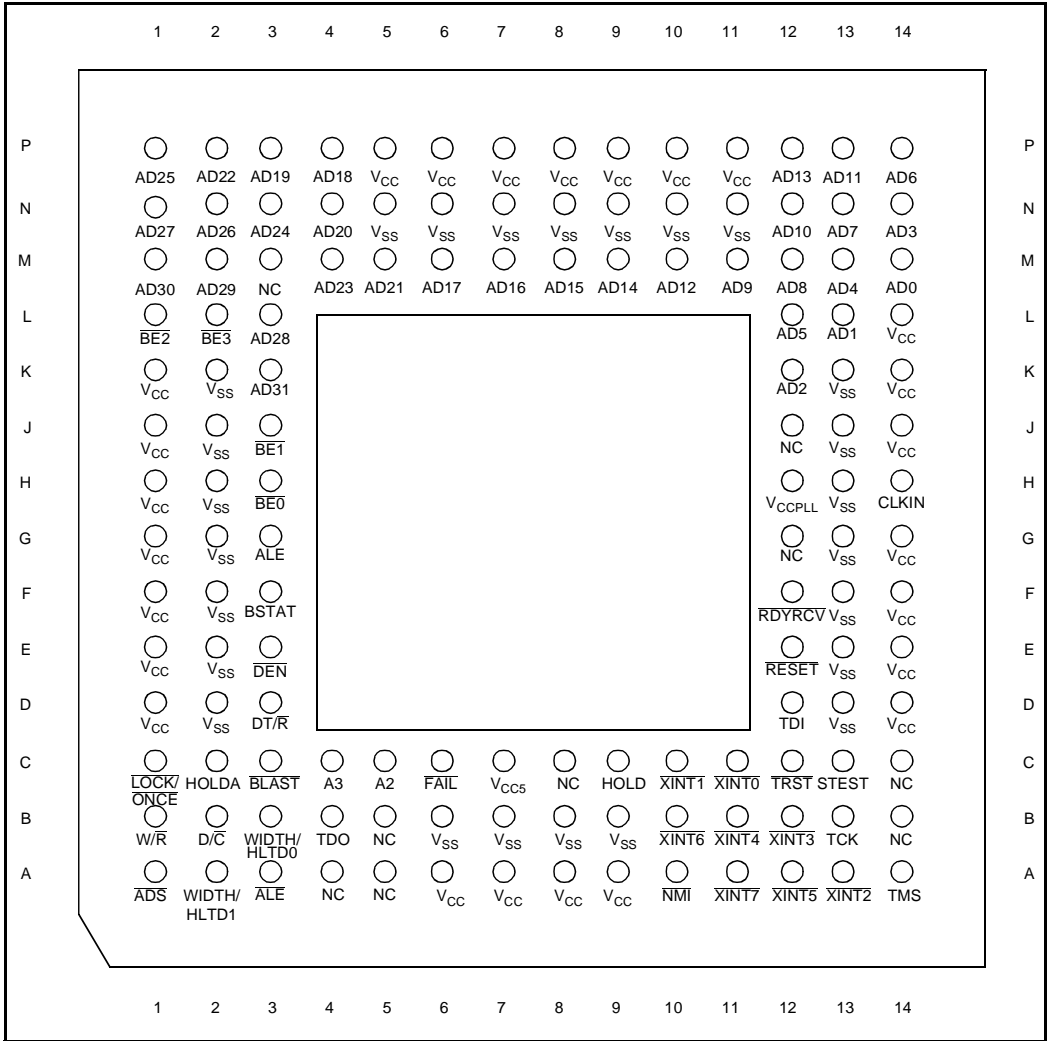


Figure 3. 132-Lead Pin Grid Array Bottom View - Pins Facing Up

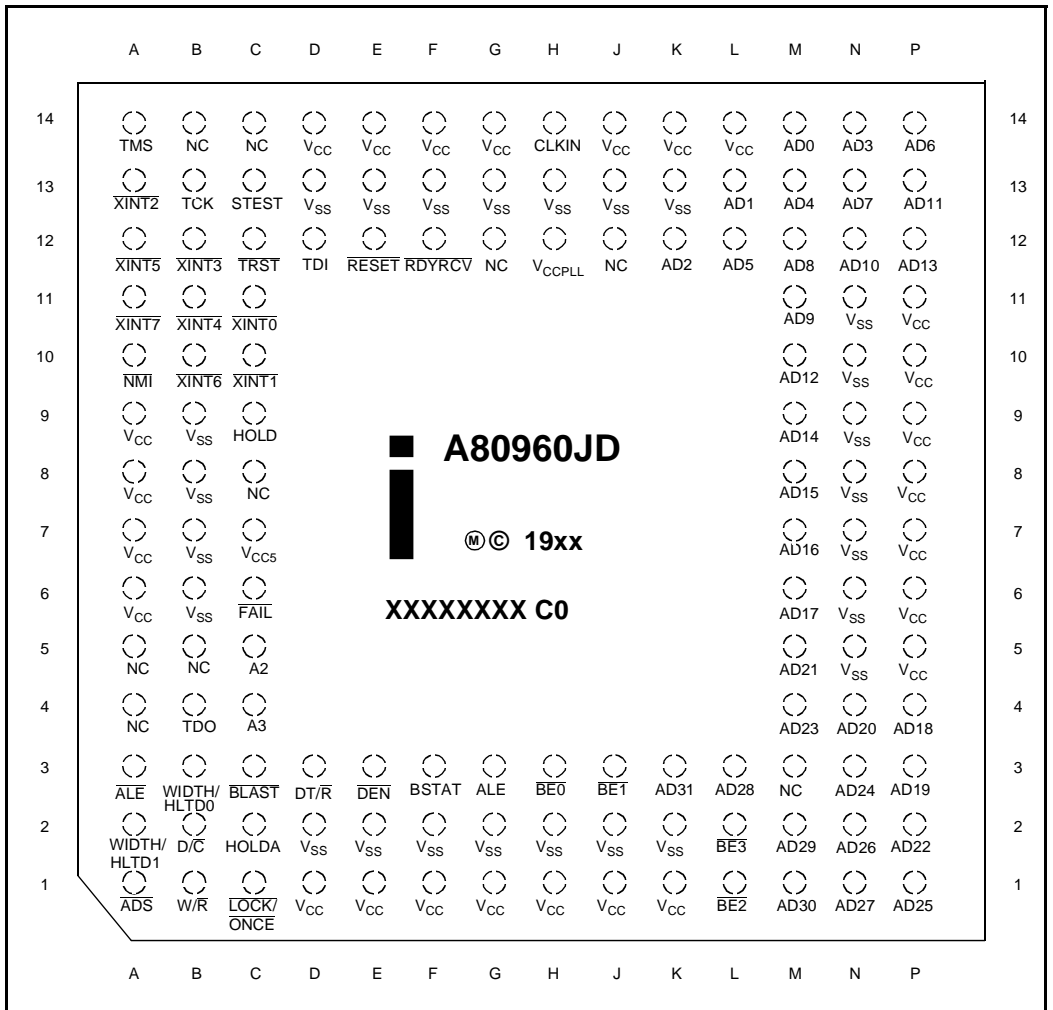


Figure 4. 132-Lead Pin Grid Array Top View - Pins Facing Down

Table 6. 132-Lead PGA Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	C5	AD31	K3	TDO	B4	V _{SS}	B9
A3	C4	ADS	A1	TMS	A14	V _{SS}	D2
AD0	M14	ALE	G3	TRST	C12	V _{SS}	D13
AD1	L13	ĀLE	A3	V _{CC}	A6	V _{SS}	E2
AD2	K12	BE0	H3	V _{CC}	A7	V _{SS}	E13
AD3	N14	BE1	J3	V _{CC}	A8	V _{SS}	F2
AD4	M13	BE2	L1	V _{CC}	A9	V _{SS}	F13
AD5	L12	BE3	L2	V _{CC}	D1	V _{SS}	G2
AD6	P14	BLAST	C3	V _{CC}	D14	V _{SS}	G13
AD7	N13	BSTAT	F3	V _{CC}	E1	V _{SS}	H2
AD8	M12	CLKIN	H14	V _{CC}	E14	V _{SS}	H13
AD9	M11	D/C	B2	V _{CC}	F1	V _{SS}	J2
AD10	N12	DĒN	E3	V _{CC}	F14	V _{SS}	J13
AD11	P13	DT/R	D3	V _{CC}	G1	V _{SS}	K2
AD12	M10	FAIL	C6	V _{CC}	G14	V _{SS}	K13
AD13	P12	HOLD	C9	V _{CC}	H1	V _{SS}	N5
AD14	M9	HOLDA	C2	V _{CC}	J1	V _{SS}	N6
AD15	M8	LOCK/ONCE	C1	V _{CC}	J14	V _{SS}	N7
AD16	M7	NC	A4	V _{CC}	K1	V _{SS}	N8
AD17	M6	NC	A5	V _{CC}	K14	V _{SS}	N9
AD18	P4	NC	B5	V _{CC}	L14	V _{SS}	N10
AD19	P3	NC	B14	V _{CC}	P5	V _{SS}	N11
AD20	N4	NC	C8	V _{CC}	P6	W/R	B1
AD21	M5	NC	C14	V _{CC}	P7	WIDTH/HLTD0	B3
AD22	P2	NC	G12	V _{CC}	P8	WIDTH/HLTD1	A2
AD23	M4	NC	J12	V _{CC}	P9	XINT0	C11
AD24	N3	NC	M3	V _{CC}	P10	XINT1	C10
AD25	P1	NMI	A10	V _{CC}	P11	XINT2	A13
AD26	N2	RDYRCV	F12	V _{CC} PLL	H12	XINT3	B12
AD27	N1	RESET	E12	V _{CC} 5	C7	XINT4	B11
AD28	L3	STEST	C13	V _{SS}	B6	XINT5	A12
AD29	M2	TCK	B13	V _{SS}	B7	XINT6	B10
AD30	M1	TDI	D12	V _{SS}	B8	XINT7	A11

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 7. 132-Lead PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	ADS	C6	FAIL	H1	V _{CC}	M10	AD12
A2	WIDTH/HLTD1	C7	V _{CC5}	H2	V _{SS}	M11	AD9
A3	ALE	C8	NC	H3	BE ₀	M12	AD8
A4	NC	C9	HOLD	H12	V _{CCPLL}	M13	AD4
A5	NC	C10	XINT1	H13	V _{SS}	M14	AD0
A6	V _{CC}	C11	XINT0	H14	CLKIN	N1	AD27
A7	V _{CC}	C12	TRST	J1	V _{CC}	N2	AD26
A8	V _{CC}	C13	STEST	J2	V _{SS}	N3	AD24
A9	V _{CC}	C14	NC	J3	BE ₁	N4	AD20
A10	NMI	D1	V _{CC}	J12	NC	N5	V _{SS}
A11	XINT7	D2	V _{SS}	J13	V _{SS}	N6	V _{SS}
A12	XINT5	D3	DT/R	J14	V _{CC}	N7	V _{SS}
A13	XINT2	D12	TDI	K1	V _{CC}	N8	V _{SS}
A14	TMS	D13	V _{SS}	K2	V _{SS}	N9	V _{SS}
B1	W/R	D14	V _{CC}	K3	AD31	N10	V _{SS}
B2	D/C	E1	V _{CC}	K12	AD2	N11	V _{SS}
B3	WIDTH/HLTD0	E2	V _{SS}	K13	V _{SS}	N12	AD10
B4	TDO	E3	DE _N	K14	V _{CC}	N13	AD7
B5	NC	E12	RESET	L1	BE ₂	N14	AD3
B6	V _{SS}	E13	V _{SS}	L2	BE ₃	P1	AD25
B7	V _{SS}	E14	V _{CC}	L3	AD28	P2	AD22
B8	V _{SS}	F1	V _{CC}	L12	AD5	P3	AD19
B9	V _{SS}	F2	V _{SS}	L13	AD1	P4	AD18
B10	XINT6	F3	BSTAT	L14	V _{CC}	P5	V _{CC}
B11	XINT4	F12	RDYRCV	M1	AD30	P6	V _{CC}
B12	XINT3	F13	V _{SS}	M2	AD29	P7	V _{CC}
B13	TCK	F14	V _{CC}	M3	NC	P8	V _{CC}
B14	NC	G1	V _{CC}	M4	AD23	P9	V _{CC}
C1	LOCK/ONCE	G2	V _{SS}	M5	AD21	P10	V _{CC}
C2	HOLDA	G3	ALE	M6	AD17	P11	V _{CC}
C3	BLAST	G12	NC	M7	AD16	P12	AD13
C4	A3	G13	V _{SS}	M8	AD15	P13	AD11
C5	A2	G14	V _{CC}	M9	AD14	P14	AD6

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.1.3 80960Jx PQFP Pinout

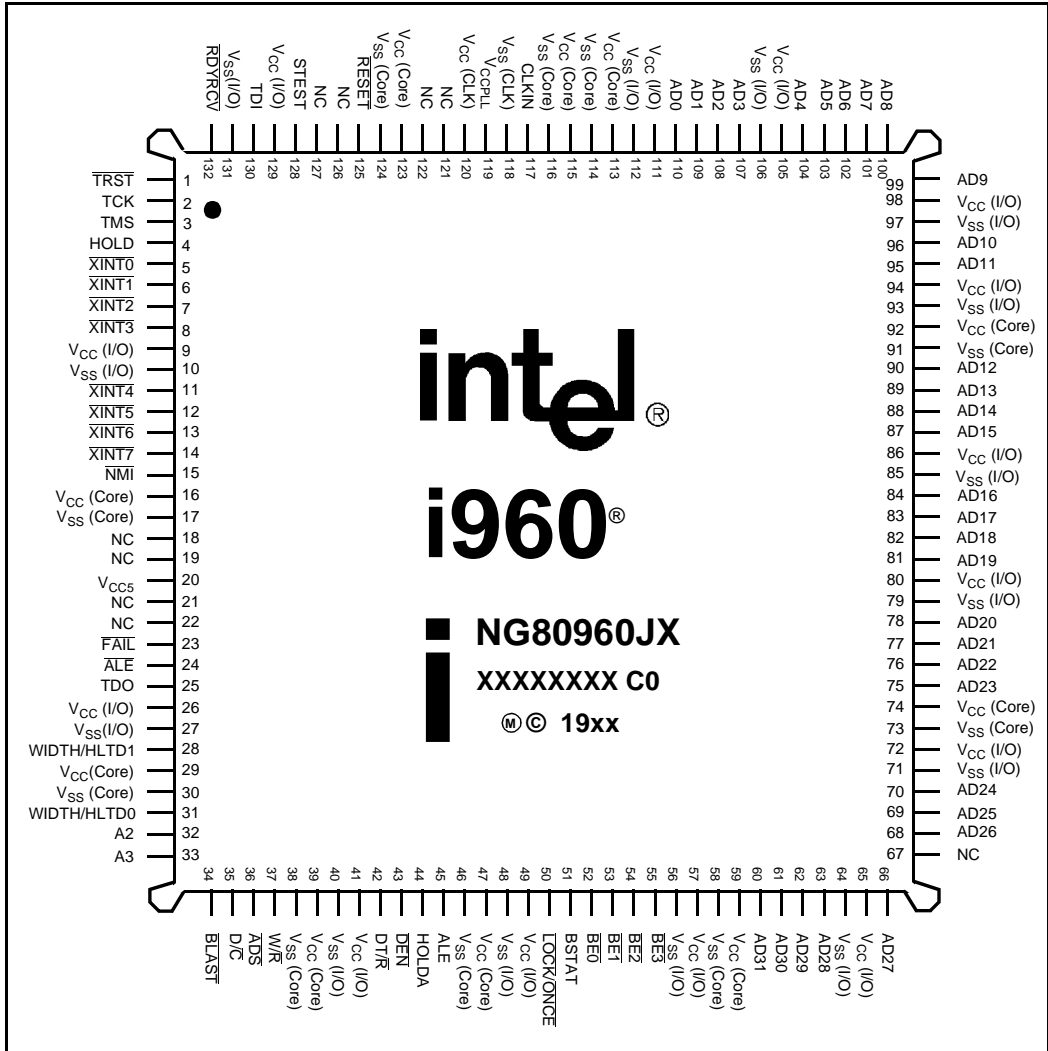


Figure 5. 132-Lead PQFP - Top View

Table 8. 132-Lead PQFP Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD31	60	\overline{ALE}	24	V_{CC} (Core)	47	V_{SS} (Core)	124
AD30	61	\overline{ADS}	36	V_{CC} (Core)	59	V_{SS} (I/O)	10
AD29	62	A3	33	V_{CC} (Core)	74	V_{SS} (I/O)	27
AD28	63	A2	32	V_{CC} (Core)	92	V_{SS} (I/O)	40
AD27	66	$\overline{BE3}$	55	V_{CC} (Core)	113	V_{SS} (I/O)	48
AD26	68	$\overline{BE2}$	54	V_{CC} (Core)	115	V_{SS} (I/O)	56
AD25	69	$\overline{BE1}$	53	V_{CC} (Core)	123	V_{SS} (I/O)	64
AD24	70	$\overline{BE0}$	52	V_{CC} (I/O)	9	V_{SS} (I/O)	71
AD23	75	WIDTH/HLTD1	28	V_{CC} (I/O)	26	V_{SS} (I/O)	79
AD22	76	WIDTH/HLTD0	31	V_{CC} (I/O)	41	V_{SS} (I/O)	85
AD21	77	D/\overline{C}	35	V_{CC} (I/O)	49	V_{SS} (I/O)	93
AD20	78	W/\overline{R}	37	V_{CC} (I/O)	57	V_{SS} (I/O)	97
AD19	81	DT/\overline{R}	42	V_{CC} (I/O)	65	V_{SS} (I/O)	106
AD18	82	\overline{DEN}	43	V_{CC} (I/O)	72	V_{SS} (I/O)	112
AD17	83	\overline{BLAST}	34	V_{CC} (I/O)	80	V_{SS} (I/O)	131
AD16	84	\overline{RDYRCV}	132	V_{CC} (I/O)	86	NC	18
AD15	87	$\overline{LOCK/ONCE}$	50	V_{CC} (I/O)	94	NC	19
AD14	88	HOLD	4	V_{CC} (I/O)	98	NC	21
AD13	89	HOLDA	44	V_{CC} (I/O)	105	NC	22
AD12	90	BSTAT	51	V_{CC} (I/O)	111	NC	67
AD11	95	CLKIN	117	V_{CC} (I/O)	129	NC	121
AD10	96	\overline{RESET}	125	V_{CCPLL}	119	NC	122
AD9	99	STEST	128	V_{CC5}	20	NC	126
AD8	100	\overline{FAIL}	23	V_{SS} (CLK)	118	NC	127
AD7	101	TCK	2	V_{SS} (Core)	17	$\overline{XINT7}$	14
AD6	102	TDI	130	V_{SS} (Core)	30	$\overline{XINT6}$	13
AD5	103	TDO	25	V_{SS} (Core)	38	$\overline{XINT5}$	12
AD4	104	\overline{TRST}	1	V_{SS} (Core)	46	$\overline{XINT4}$	11
AD3	107	TMS	3	V_{SS} (Core)	58	$\overline{XINT3}$	8
AD2	108	V_{CC} (CLK)	120	V_{SS} (Core)	73	$\overline{XINT2}$	7
AD1	109	V_{CC} (Core)	16	V_{SS} (Core)	91	$\overline{XINT1}$	6
AD0	110	V_{CC} (Core)	29	V_{SS} (Core)	114	$\overline{XINT0}$	5
ALE	45	V_{CC} (Core)	39	V_{SS} (Core)	116	\overline{NMI}	15

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 9. 132-Lead PQFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	$\overline{\text{TRST}}$	34	$\overline{\text{BLAST}}$	67	NC	100	AD8
2	TCK	35	D/ $\overline{\text{C}}$	68	AD26	101	AD7
3	TMS	36	$\overline{\text{ADS}}$	69	AD25	102	AD6
4	HOLD	37	W/ $\overline{\text{R}}$	70	AD24	103	AD5
5	$\overline{\text{XINT0}}$	38	V _{SS} (Core)	71	V _{SS} (I/O)	104	AD4
6	$\overline{\text{XINT1}}$	39	V _{CC} (Core)	72	V _{CC} (I/O)	105	V _{CC} (I/O)
7	$\overline{\text{XINT2}}$	40	V _{SS} (I/O)	73	V _{SS} (Core)	106	V _{SS} (I/O)
8	$\overline{\text{XINT3}}$	41	V _{CC} (I/O)	74	V _{CC} (Core)	107	AD3
9	V _{CC} (I/O)	42	DT/ $\overline{\text{R}}$	75	AD23	108	AD2
10	V _{SS} (I/O)	43	$\overline{\text{DEN}}$	76	AD22	109	AD1
11	$\overline{\text{XINT4}}$	44	HOLDA	77	AD21	110	AD0
12	$\overline{\text{XINT5}}$	45	ALE	78	AD20	111	V _{CC} (I/O)
13	$\overline{\text{XINT6}}$	46	V _{SS} (Core)	79	V _{SS} (I/O)	112	V _{SS} (I/O)
14	$\overline{\text{XINT7}}$	47	V _{CC} (Core)	80	V _{CC} (I/O)	113	V _{CC} (Core)
15	NMI	48	V _{SS} (I/O)	81	AD19	114	V _{SS} (Core)
16	V _{CC} (Core)	49	V _{CC} (I/O)	82	AD18	115	V _{CC} (Core)
17	V _{SS} (Core)	50	LOCK/ $\overline{\text{ONCE}}$	83	AD17	116	V _{SS} (Core)
18	NC	51	BSTAT	84	AD16	117	CLKIN
19	NC	52	$\overline{\text{BE0}}$	85	V _{SS} (I/O)	118	V _{SS} (CLK)
20	V _{CC5}	53	$\overline{\text{BE1}}$	86	V _{CC} (I/O)	119	V _{CC} PLL
21	NC	54	$\overline{\text{BE2}}$	87	AD15	120	V _{CC} (CLK)
22	NC	55	$\overline{\text{BE3}}$	88	AD14	121	NC
23	$\overline{\text{FAIL}}$	56	V _{SS} (I/O)	89	AD13	122	NC
24	$\overline{\text{ALE}}$	57	V _{CC} (I/O)	90	AD12	123	V _{CC} (Core)
25	TDO	58	V _{SS} (Core)	91	V _{SS} (Core)	124	V _{SS} (Core)
26	V _{CC} (I/O)	59	V _{CC} (Core)	92	V _{CC} (Core)	125	RESET
27	V _{SS} (I/O)	60	AD31	93	V _{SS} (I/O)	126	NC
28	WIDTH/HLTD1	61	AD30	94	V _{CC} (I/O)	127	NC
29	V _{CC} (Core)	62	AD29	95	AD11	128	STEST
30	V _{SS} (Core)	63	AD28	96	AD10	129	V _{CC} (I/O)
31	WIDTH/HLTD0	64	V _{SS} (I/O)	97	V _{SS} (I/O)	130	TDI
32	A2	65	V _{CC} (I/O)	98	V _{CC} (I/O)	131	V _{SS} (I/O)
33	A3	66	AD27	99	AD9	132	RDYRCV

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.2 Package Thermal Specifications

The 80960JD is specified for operation when T_C (case temperature) is within the range of 0°C to 100°C for both PGA and PQFP packages. Case temperature may be measured in any environment to determine whether the 80960JD is within its specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

θ_{CA} is the thermal resistance from case to ambient. Use the following equation to calculate T_A , the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Junction temperature (T_J) is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P (\theta_{JC})$$

Similarly, if T_A is known, the corresponding case temperature (T_C) can be calculated as follows:

$$T_C = T_A + P (\theta_{CA})$$

Compute P by multiplying I_{CC} from Table 14 and V_{CC} . Values for θ_{JC} and θ_{CA} are given in Table 10 for the PGA package and Table 11 for the PQFP package. For high speed operation, the processor's θ_{JA} may be significantly reduced by adding a heatsink and/or by increasing airflow.

Table 12 shows the maximum ambient temperature (T_A) permitted without exceeding T_C for both PGA and PQFP packages. The values are based on typical I_{CC} and V_{CC} of +3.3 V, with a T_{CASE} of +100°C.

Table 10. 132-Lead PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	0.7	0.7	0.7	0.7	0.7	0.7
θ_{CA} (Case-to-Ambient) (No Heatsink)	25	19	14	12	11	10
θ_{CA} (Case-to-Ambient) (Omnidirectional Heatsink)	15	9	6	5	4	4
θ_{CA} (Case-to-Ambient) (Unidirectional Heatsink)	16	8	6	5	4	4

NOTES:

1. This table applies to a PGA device plugged into a socket or soldered directly into a board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{J-CAP} = 5.6^\circ\text{C/W}$ (approx.) (no heatsink)
4. $\theta_{J-PIN} = 6.4^\circ\text{C/W}$ (inner pins) (approx.) (no heatsink)
5. $\theta_{J-PIN} = 6.2^\circ\text{C/W}$ (outer pins) (approx.) (no heatsink)
6. $\theta_{J-CAP} = 3^\circ\text{C/W}$ (approx.) (with heatsink)
7. $\theta_{J-PIN} = 3.3^\circ\text{C/W}$ (inner pins) (approx.) (with heatsink)
8. $\theta_{J-PIN} = 3.3^\circ\text{C/W}$ (outer pins) (approx.) (with heatsink)

Table 11. 132-Lead PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt								
Parameter	Airflow — ft./min (m/sec)							
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	4.1	4.3	4.3	4.3	4.3	4.7	4.9	5.3
θ_{CA} (Case-to-Ambient -No Heatsink)	23	19	18	16	14	11	9	8

NOTES:

1. This table applies to a PQFP device soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{JL} = 13^{\circ}\text{C/W}$ (approx.)
4. $\theta_{JB} = 13.5^{\circ}\text{C/W}$ (approx.)

Table 12. Maximum T_A at Various Airflows in °C

		f_{CLKIN} (MHz)	Airflow-ft/min (m/sec)					
			0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
PQFP Package	T_A without Heatsink	66	61	73	76	81	85	86
		50	70	79	82	86	88	90
		40	77	84	86	89	91	92
PGA Package	T_A without Heatsink	66	58	68	76	80	81	83
		50	68	75	82	84	86	87
		40	75	81	86	88	89	90
	T_A with Omni Heatsink ¹	66	75	85	90	92	93	93
		50	81	88	92	94	95	95
		40	85	91	94	95	96	96
	T_A with Uni-directional Heatsink ²	66	73	86	90	92	93	93
		50	79	90	92	94	95	95
		40	84	92	94	95	96	96

1. 0.248" high omnidirectional heatsink (Al alloy 6061, 41mil fin width, 124 mil center-to-center fin spacing)

2. 0.250" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 146 mil center-to-center fin spacing)

3.3 Thermal Management Accessories

The following is a list of suggested sources for 80960JD thermal solutions. This is neither an endorsement or a warranty of the performance of any of the listed products and/or companies.

Heatsinks

1. Thermalloy, Inc.
2021 West Valley View Lane
Dallas, TX 75234-8993
(214) 243-4321 FAX: (214) 241-4656
2. Wakefield Engineering
60 Audubon Road
Wakefield, MA 01880
(617) 245-5900
3. Aavid Thermal Technologies, Inc.
One Kool Path
Laconia, NH 03247-0400
(603) 528-3400

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	-65°C to +150°C
Case Temperature Under Bias	-65°C to +110°C
Supply Voltage wrt. V_{SS}	-0.5 V to + 4.6 V
Voltage on V_{CC5} wrt. V_{SS}	-0.5 V to + 6.5 V
Voltage on Other Pins wrt. V_{SS}	-0.5 V to $V_{CC} + 0.5$ V

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

WARNING: *Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

4.2 Operating Conditions

Table 13. 80960JD Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.15	3.45	V	
V_{CC5}	Input Protection Bias	3.15	5.5	V	(1)
f_{CLKIN}	Input Clock Frequency				
	80960JD-66	12	33.3	MHz	
	80960JD-50	12	25		
	80960JD-40	12	20		
T_C	Operating Case Temperature (PGA and PQFP)	0	100	°C	

NOTES:

1. See Section 4.4, V_{CC5} Pin Requirements (V_{DIFF}) (pg. 23)

4.3 Connection Recommendations

For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960JD power and ground pins. On the circuit board, every V_{CC} pin should connect to a power plane and every V_{SS} pin should connect to a ground plane. Place liberal decoupling capacitance near the 80960JD, since the processor can cause transient power surges.

Pay special attention to the Test Reset (\overline{TRST}) pin. It is essential that the JTAG Boundary Scan Test Access Port (TAP) controller initializes to a known state whether it will be used or not. If the JTAG Boundary Scan function will be used, connect a pulldown resistor between the \overline{TRST} pin and V_{SS} . If the JTAG Boundary Scan function will not be used (even for board-level testing), connect the \overline{TRST} pin to V_{SS} . Also, do not connect the TDI, TDO, and TCK pins if the TAP Controller will not be used.

Pins identified as NC must not be connected in the system.

4.4 V_{CC5} Pin Requirements (V_{DIFF})

In mixed voltage systems where the processor is powered by 3.3 volts and interfaces with 5 volt components, V_{CC5} must be connected to 5 volts. This allows proper 5 volt tolerant buffer operation, and prevents damage to the input pins. The voltage differential between the 80960Jx V_{CC5} pin and its 3.3 volt V_{CC} pins must not exceed 2.25 volts. If this requirement is not met, current flow through the pin may exceed the value at which the processor is damaged. Instances when the voltage can exceed 2.25 volts is during power up or power down, where one source reaches its level faster than the other, briefly causing an excess voltage differential. Another instance is during steady-state operation, where the differential voltage of the regulator (provided a regulator is used) cannot be maintained within 2.25 volts. Two methods are possible to prevent this from happening:

- Use a regulator that is designed to prevent the voltage differential from exceeding 2.25 volts, or,

As shown in Figure 6, place a 100 Ω resistor in series with the V_{CC5} pin to limit the current through V_{CC5} .

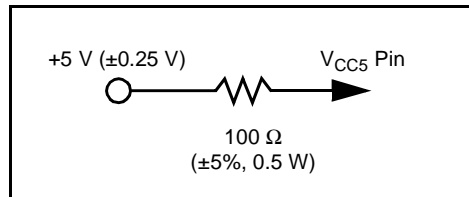


Figure 6. V_{CC5} Current-Limiting Resistor

- If the regulator cannot prevent the 2.25 volt differential, the addition of the resistor is a simple and reliable method for limiting current. The resistor can also prevent damage in the case of a power failure, where the 5 volt supply remains on and the 3.3 volt supply goes to zero.

In 3.3 volt only systems where the 80960Jx input pins are driven from 3.3 volt logic, connect the V_{CC5} pin directly to the 3.3 volt V_{CC} plane.

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	$V_{CC5}-V_{CC}$ Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25 V during power-up and power-down, or during steady-state operation.

4.5 V_{CCPLL} Pin Requirements

To reduce clock jitter on the i960 Jx processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The lowpass filter, as shown in Figure 7, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 4.7 μ F capacitor must be of the type

tantalum), the 0.01 μ F capacitor must be of the type X7R and the node connecting V_{CCPLL} must be as short as possible.

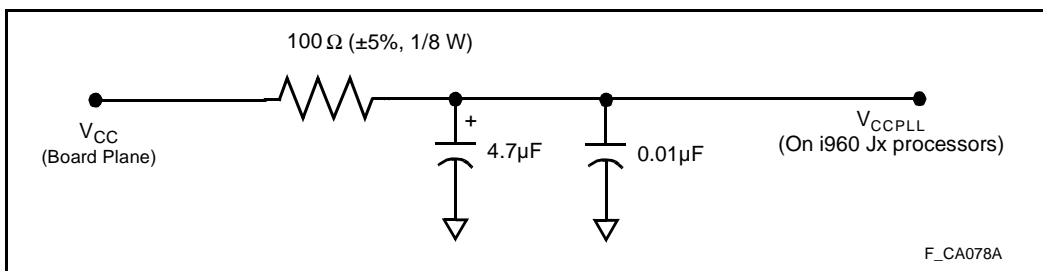


Figure 7. V_{CCPLL} Lowpass Filter

4.6 DC Specifications

Table 14. 80960JD DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC5} + 0.3$	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 3 \text{ mA}$
				0.2	V	$I_{OL} = 100 \mu\text{A}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -1 \text{ mA}$
		$V_{CC} - 0.2$				$I_{OH} = -200 \mu\text{A}$
V_{OLP}	Output Ground Bounce		TBD		V	(1,2)
C_{IN}	Input Capacitance PGA PQFP			15	pF	$f_{CLKIN} = f_{MIN} (2)$
				15		
C_{OUT}	I/O or Output Capacitance PGA PQFP			15	pF	$f_{CLKIN} = f_{MIN} (2)$
				15		
C_{CLK}	CLKIN Capacitance PGA PQFP			15	pF	$f_{CLKIN} = f_{MIN} (2)$
				15		

NOTES:

1. Typical is measured with $V_{CC} = 3.3 \text{ V}$ and temperature = $25 \text{ }^\circ\text{C}$.
2. Not tested.

Table 15. 80960JD I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes	
I _{LI1}	Input Leakage Current for each pin except TCK, TDI, TRST and TMS		± 1	μA	0 ≤ V _{IN} ≤ V _{CC}	
I _{LI2}	Input Leakage Current for TCK, TDI, TRST and TMS	-140	-250	μA	V _{IN} = 0.45V (1)	
I _{LO}	Output Leakage Current		± 1	μA	0.4 ≤ V _{OUT} ≤ V _{CC}	
R _{pu}	Internal Pull-UP Resistance for ONCE, TMS, TDI and TRST	20	30	kΩ		
I _{CC} Active (Power Supply)	80960JD-66		790	mA	(2,3)	
	80960JD-50		600		(2,3)	
	80960JD-40		500		(2,3)	
I _{CC} Active (Thermal)	80960JD-66	720		mA	(2,4)	
	80960JD-50	540			(2,4)	
	80960JD-40	435			(2,4)	
I _{CC} Test (Power modes)	Reset mode			mA		
	80960JD-66		703		(5)	
	80960JD-50		535		(5)	
	80960JD-40		430		(5)	
	Halt mode					
	80960JD-66		61		(5)	
	80960JD-50		49		(5)	
80960JD-40		41	(5)			
ONCE mode			10	(5)		
I _{CC5} Current on the V _{CC5} Pin	80960JD-66		200	μA	(6)	
	80960JD-50		200			
	80960JD-40		200			

4.7 AC Specifications

The 80960JD AC timings are based upon device characterization.

Table 16. 80960JD AC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
INPUT CLOCK TIMINGS					
T _F	CLKIN Frequency				
	80960JD-66	12	33.3	MHz	
	80960JD-50	12	25		
80960JD-40	12	20			
T _c	CLKIN Period			ns	
	80960JD-66	30	83.3		
	80960JD-50	40	83.3		
	80960JD-40	12	83.3		
T _{CS}	CLKIN Period Stability		± 250	ps	(1, 2)
T _{CH}	CLKIN High Time	8		ns	Measured at 1.5 V (1)
T _{CL}	CLKIN Low Time	8		ns	Measured at 1.5 V (1)
T _{CR}	CLKIN Rise Time		4	ns	0.8 V to 2.0 V (1)
T _{CF}	CLKIN Fall Time		4	ns	2.0 V to 0.8 V (1)
SYNCHRONOUS OUTPUT TIMINGS					
T _{OV1}	Output Valid Delay, Except ALE/ALE Inactive and DT/R for 3.3V input signals.	2.5	13.5	ns	(3)
	Same as above, but for 5.5V input signals.	2.5	16.5		
T _{OV2}	Output Valid Delay, DT/R	0.5T _C + 7	0.5T _C + 9	ns	
T _{OF}	Output Float Delay	2.5	13.5	ns	(4)
SYNCHRONOUS INPUT TIMINGS					
T _{IS1}	Input Setup to CLKIN — AD31:0, NMI, XINT7:0	6		ns	(5)
T _{IH1}	Input Hold from CLKIN — AD31:0, NMI, XINT7:0	1.5		ns	(5)
T _{IS2}	Input Setup to CLKIN — RDYRCV and HOLD	6.5		ns	(6)
T _{IH2}	Input Hold from CLKIN — RDYRCV and HOLD	1		ns	(6)
T _{IS3}	Input Setup to CLKIN — RESET	7		ns	(7)
T _{IH3}	Input Hold from CLKIN — RESET	2		ns	(7)
T _{IS4}	Input Setup to RESET — ONCE, STEST	7		ns	(8)
T _{IH4}	Input Hold from RESET — ONCE, STEST	2		ns	(8)

NOTES: See Table 17 on page 28 for note definitions for this table.

Table 16. 80960JD AC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
RELATIVE OUTPUT TIMINGS					
T_{LX}	Address Valid to ALE/ALE Inactive	$0.5T_C - 5$			
T_{LXL}	ALE/ALE Width	$0.5T_C - 7$		ns	(9)
T_{LXA}	Address Hold from ALE/ALE Inactive				Equal Loading (9)
T_{DXD}	DT/R Valid to DEN Active				Equal Loading (9)
BOUNDARY SCAN TEST SIGNAL TIMINGS					
T_{BSF}	TCK Frequency		$0.5T_F$	MHz	
T_{BSCH}	TCK High Time	15		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	15		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	4		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	6		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	(1,10)
T_{BSOF1}	TDO Float Delay	3	30	ns	(1,10)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	(1,10)
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	30	ns	(1,10)
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	4		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	6		ns	

NOTES: See Table 17 on page 28 for note definitions for this table.

Table 17. Note Definitions for Table 16, 80960JD AC Characteristics (pg. 26)

NOTES:

1. Not tested.
2. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal clock, the jitter frequency spectrum should not have any power peaking between 500 KHz and 1/3 of the CLKIN frequency.
3. Inactive ALE/ $\overline{\text{ALE}}$ refers to the falling edge of ALE and the rising edge of $\overline{\text{ALE}}$. For inactive ALE/ $\overline{\text{ALE}}$ timings, refer to Relative Output Timings in this table.
4. A float condition occurs when the output current becomes less than I_{LO} . Float delay is not tested, but is designed to be no longer than the valid delay.
5. AD31:0 are synchronous inputs. Setup and hold times must be met for proper processor operation. $\overline{\text{NMI}}$ and $\overline{\text{XINT7:0}}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, $\overline{\text{NMI}}$ and $\overline{\text{XINT7:0}}$ must be asserted for a minimum of two CLKIN periods to guarantee recognition.
6. $\overline{\text{RDYRCV}}$ and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
7. $\overline{\text{RESET}}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
8. $\overline{\text{ONCE}}$ and $\overline{\text{STEST}}$ must be stable at the rising edge of $\overline{\text{RESET}}$ for proper operation.
9. Guaranteed by design. May not be 100% tested.
10. Relative to falling edge of TCK.
11. Worst-case T_{OV} condition occurs on I/O pins when pins transition from a floating high input to driving a low output state. The Address/Data Bus pins encounter this condition between the last access of a read, and the address cycle of a following write. 5 V signals take 3 ns longer to discharge than 3.3 V signals at 50 pF loads.

4.7.1 AC Test Conditions and Derating Curves

The AC Specifications in **Section 4.7, AC Specifications** are tested with the 50 pF load indicated in Figure 8. Figure 9 shows how timings vary with load capacitance; Figure 11 shows how output rise and fall times vary with load capacitance.

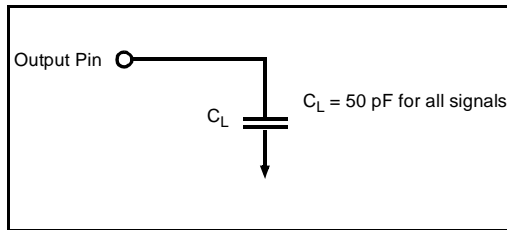


Figure 8. AC Test Load

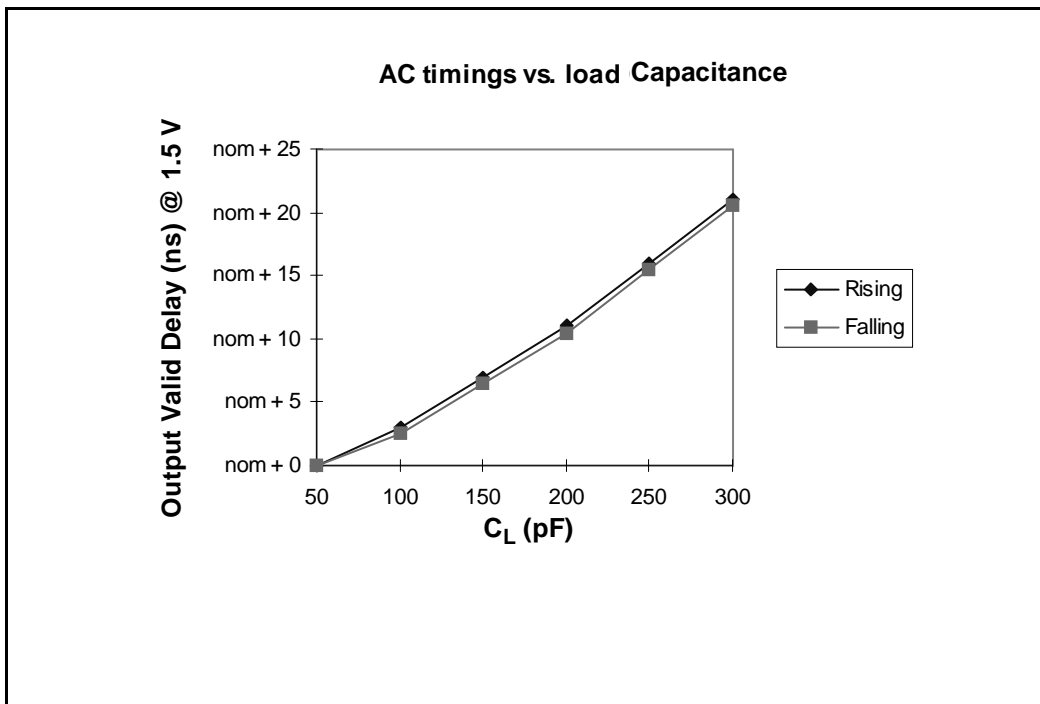


Figure 9. Output Delay or Hold vs. Load Capacitance

4.7.2 AC Timing Waveforms

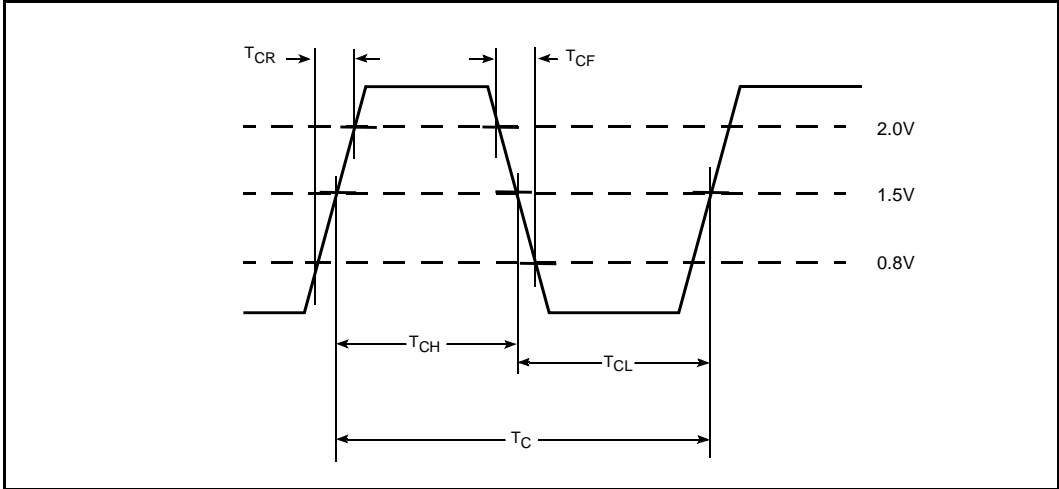


Figure 10. CLKIN Waveform

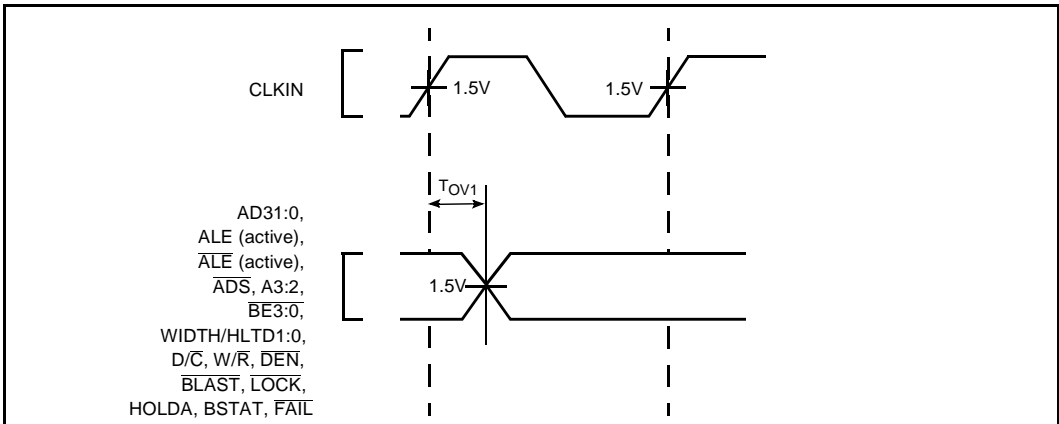


Figure 11. Output Delay Waveform for T_{OV1}

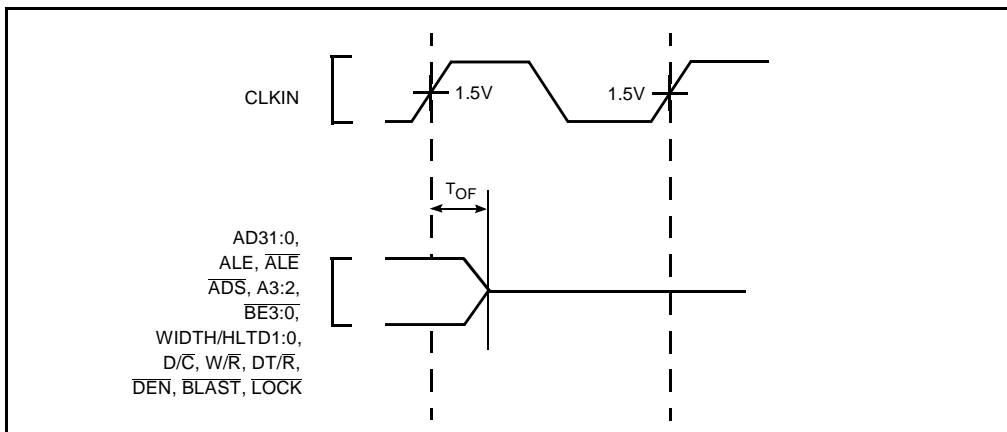


Figure 12. Output Float Waveform for T_{OF}

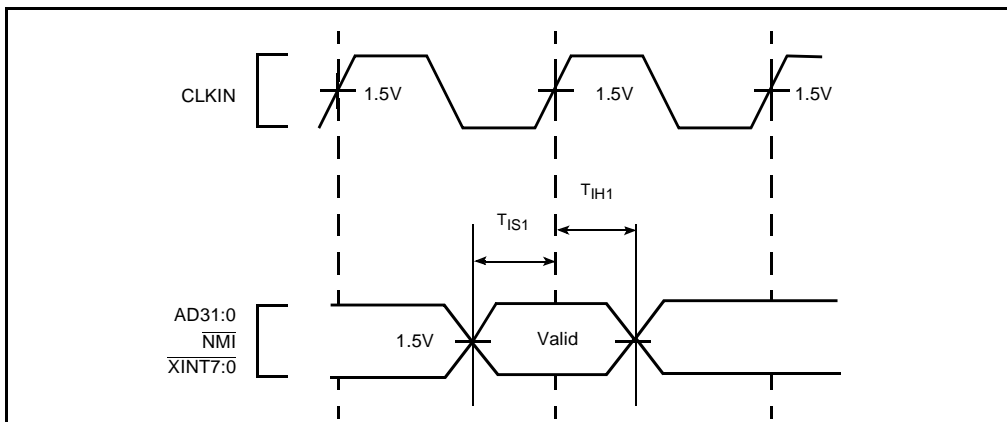


Figure 13. Input Setup and Hold Waveform for T_{IS1} and T_{IH1}

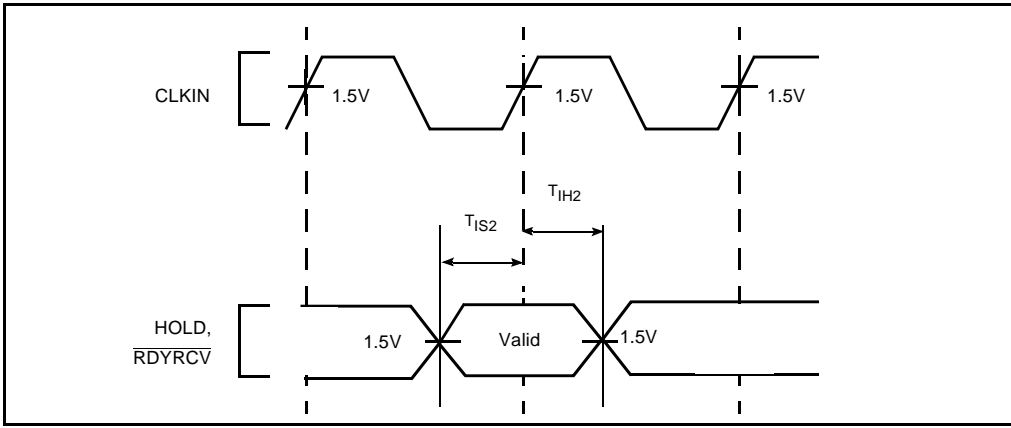


Figure 14. Input Setup and Hold Waveform for T_{IS2} and T_{IH2}

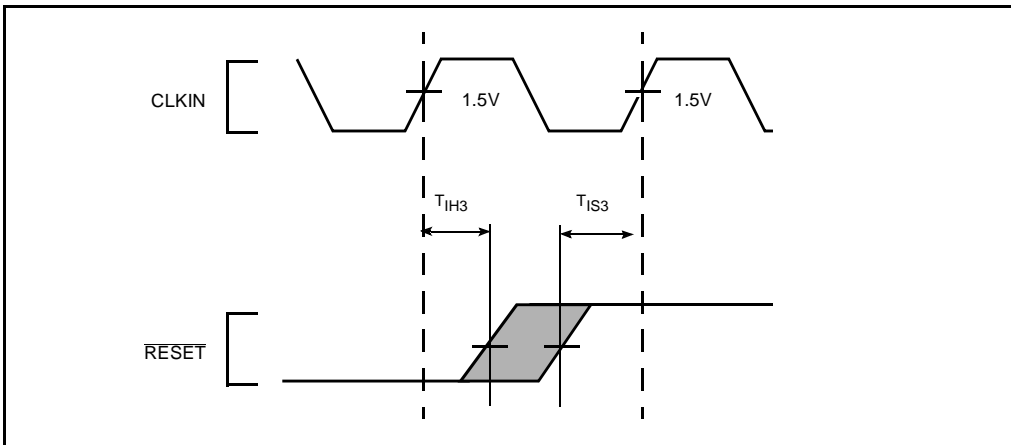


Figure 15. Input Setup and Hold Waveform for T_{IS3} and T_{IH3}

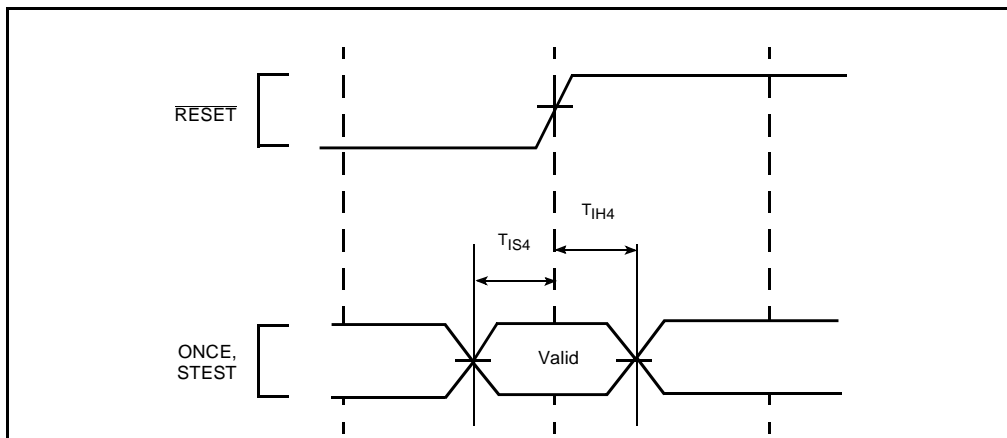


Figure 16. Input Setup and Hold Waveform for T_{IS4} and T_{IH4}

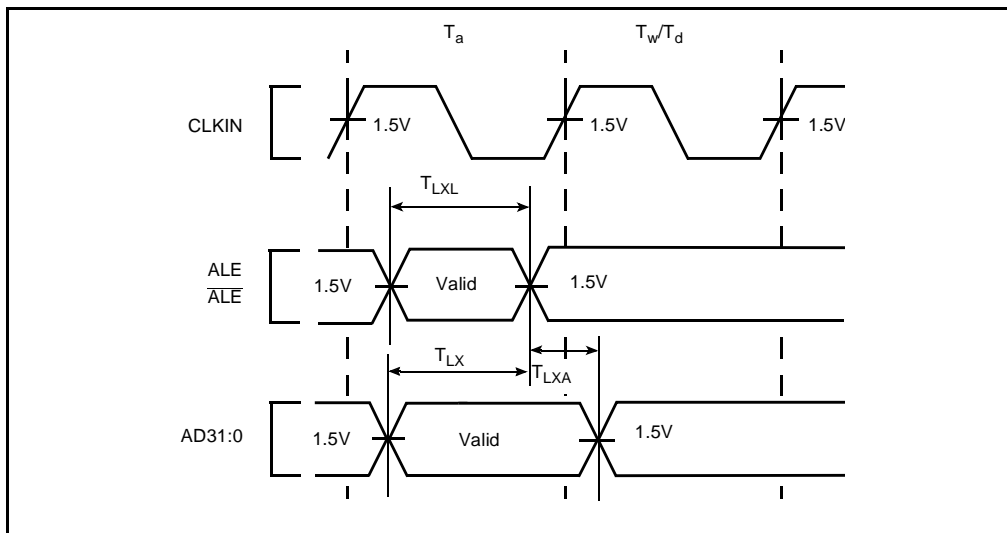


Figure 17. Relative Timings Waveform for T_{LX} , T_{LXL} and T_{LXA}

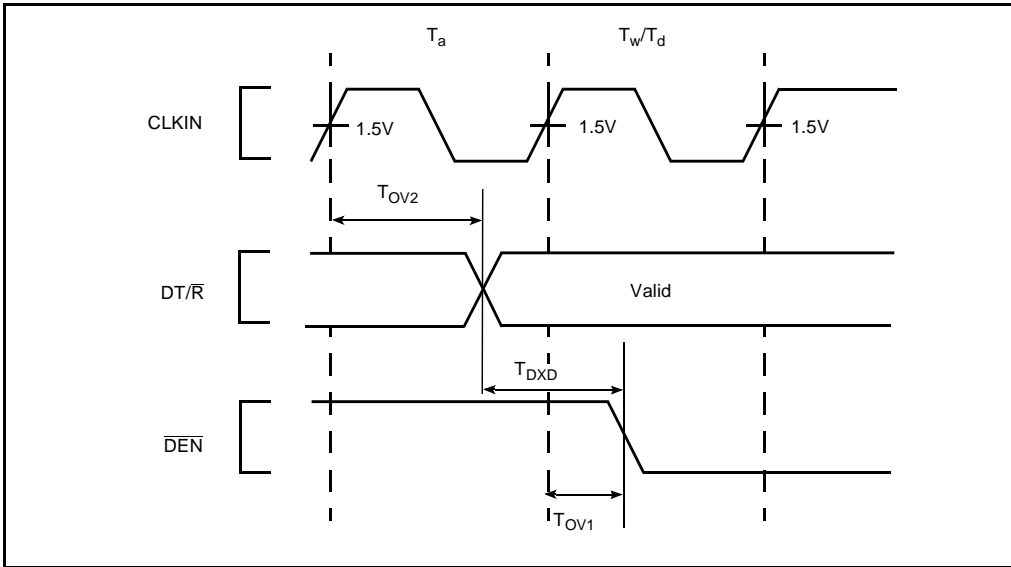


Figure 18. DT/R and DEN Timings Waveform

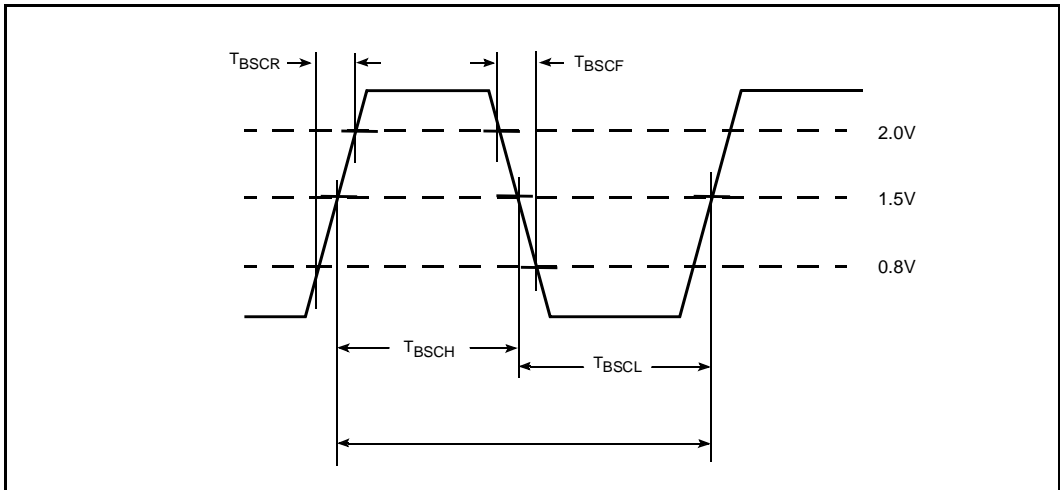


Figure 19. TCK Waveform

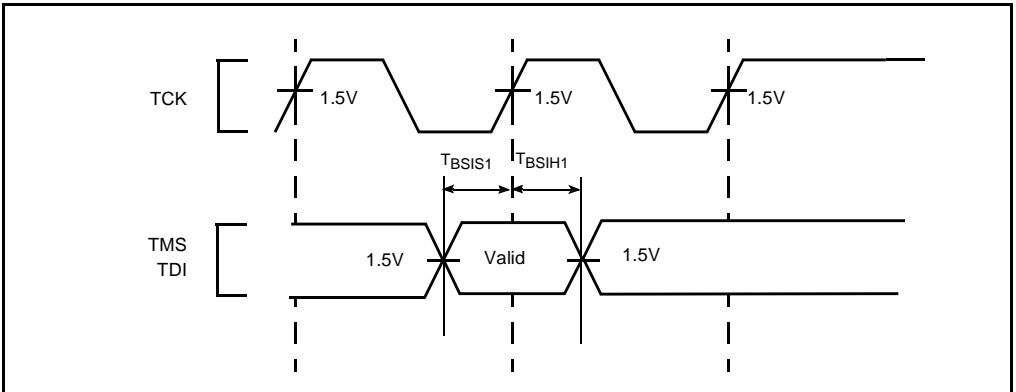


Figure 20. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

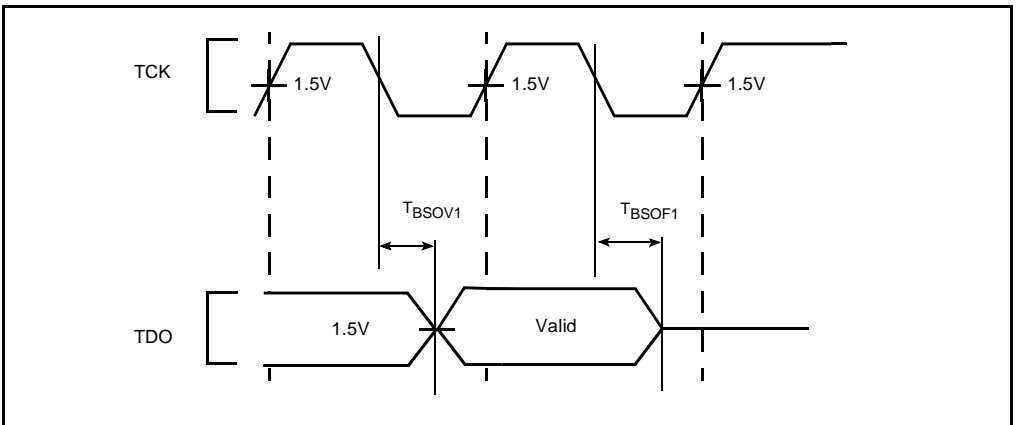


Figure 21. Output Delay and Output Float Waveform for T_{BSOV1} AND T_{BSOF1}

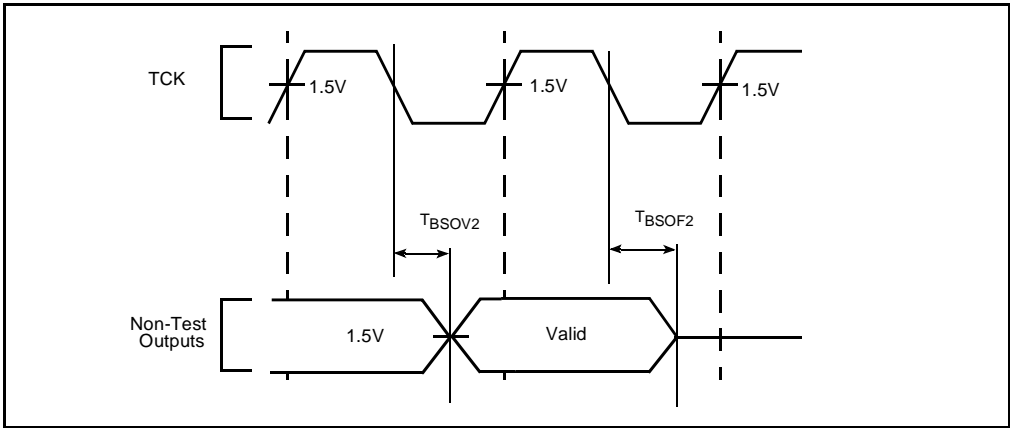


Figure 22. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}

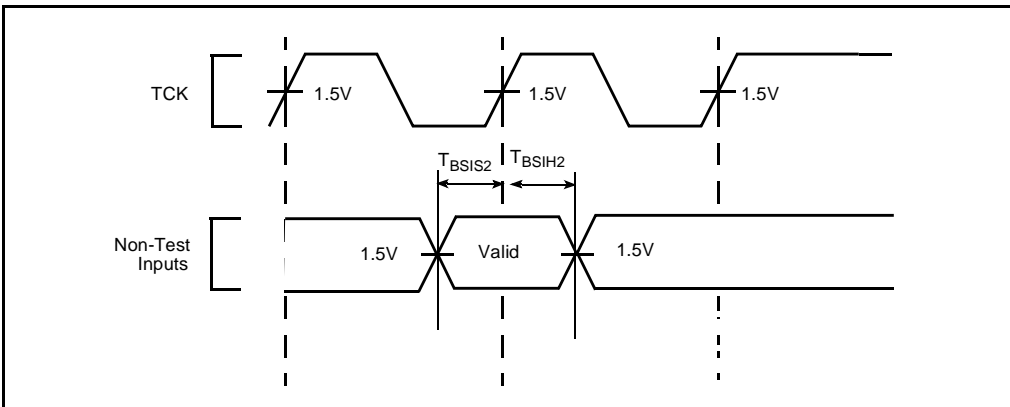


Figure 23. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}

5.0 BUS FUNCTIONAL WAVEFORMS

Figures 24 through 29 illustrate typical 80960JD bus transactions. Figure 30 depicts the bus arbitration sequence. Figure 31 illustrates the processor reset sequence from the time power is applied to the device. Figure 32 illustrates the processor reset sequence when the processor is in operation. Figure

33 illustrates the processor \overline{ONCE} sequence from the time power is applied to the device. Figures 34 and 35 also show accesses on 32-bit buses. Tables 18 through 21 summarize all possible combinations of bus accesses across 8-, 16-, and 32-bit buses according to data alignment.

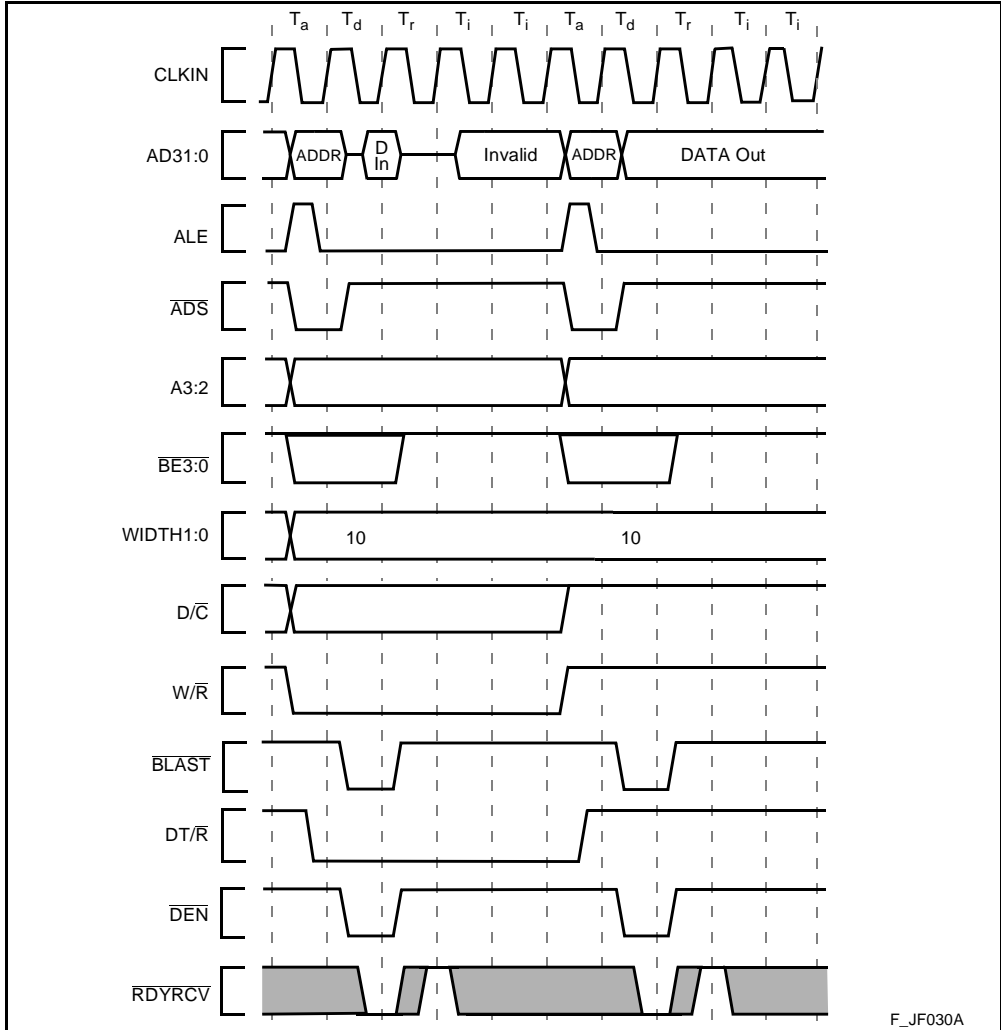


Figure 24. Non-Burst Read and Write Transactions Without Wait States, 32-Bit Bus

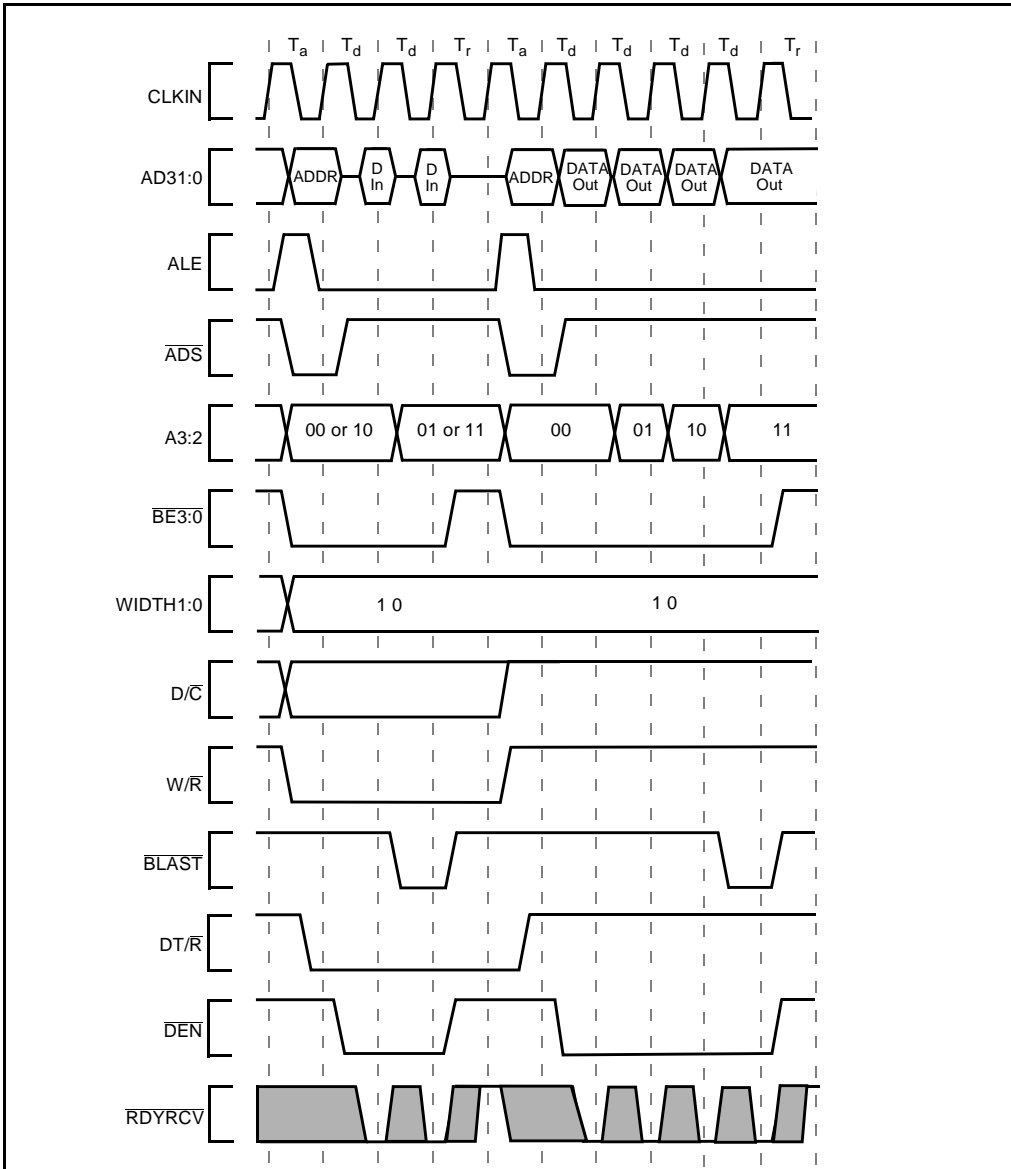


Figure 25. Burst Read and Write Transactions Without Wait States, 32-Bit Bus

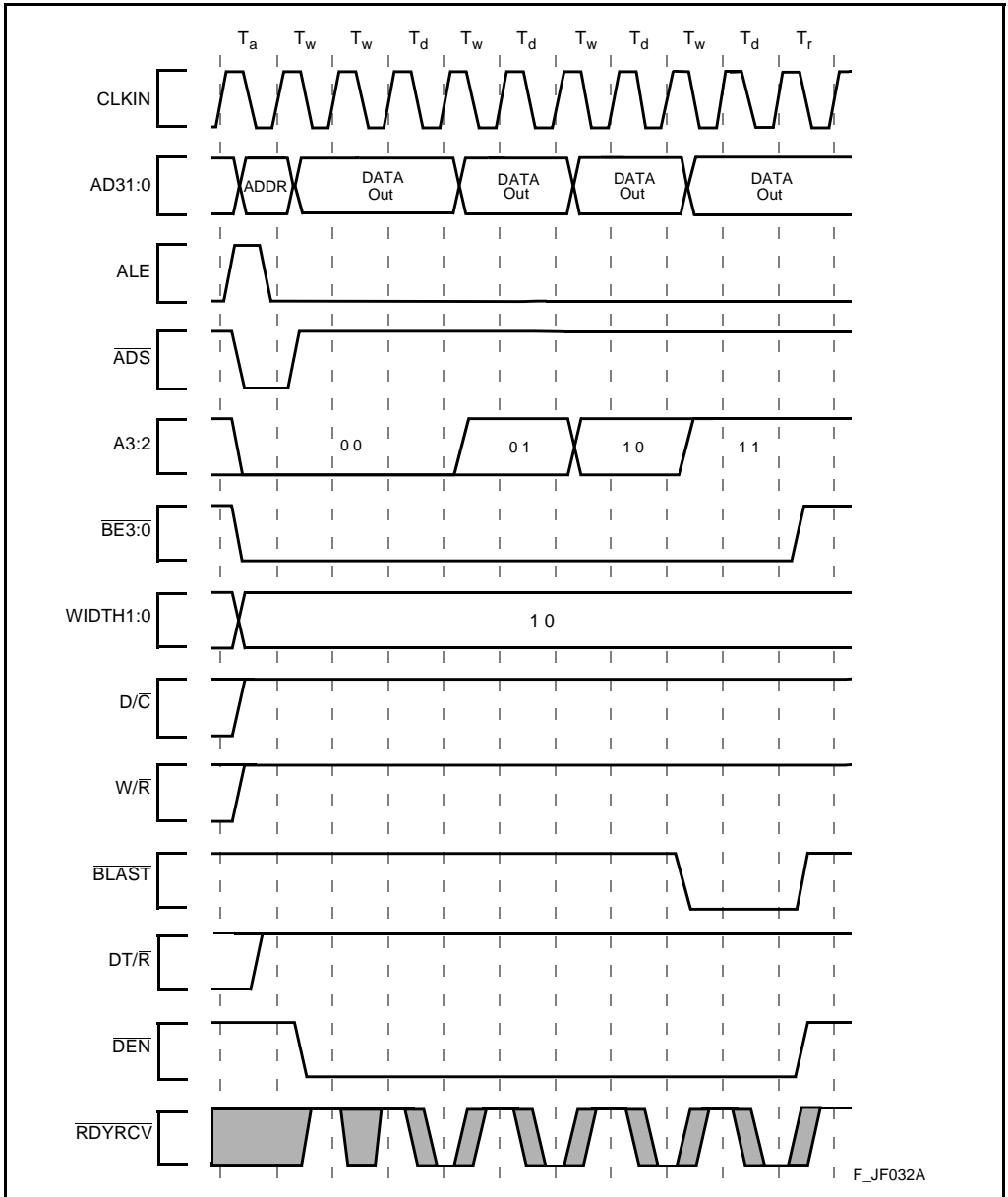


Figure 26. Burst Write Transactions With 2,1,1,1 Wait States, 32-Bit Bus

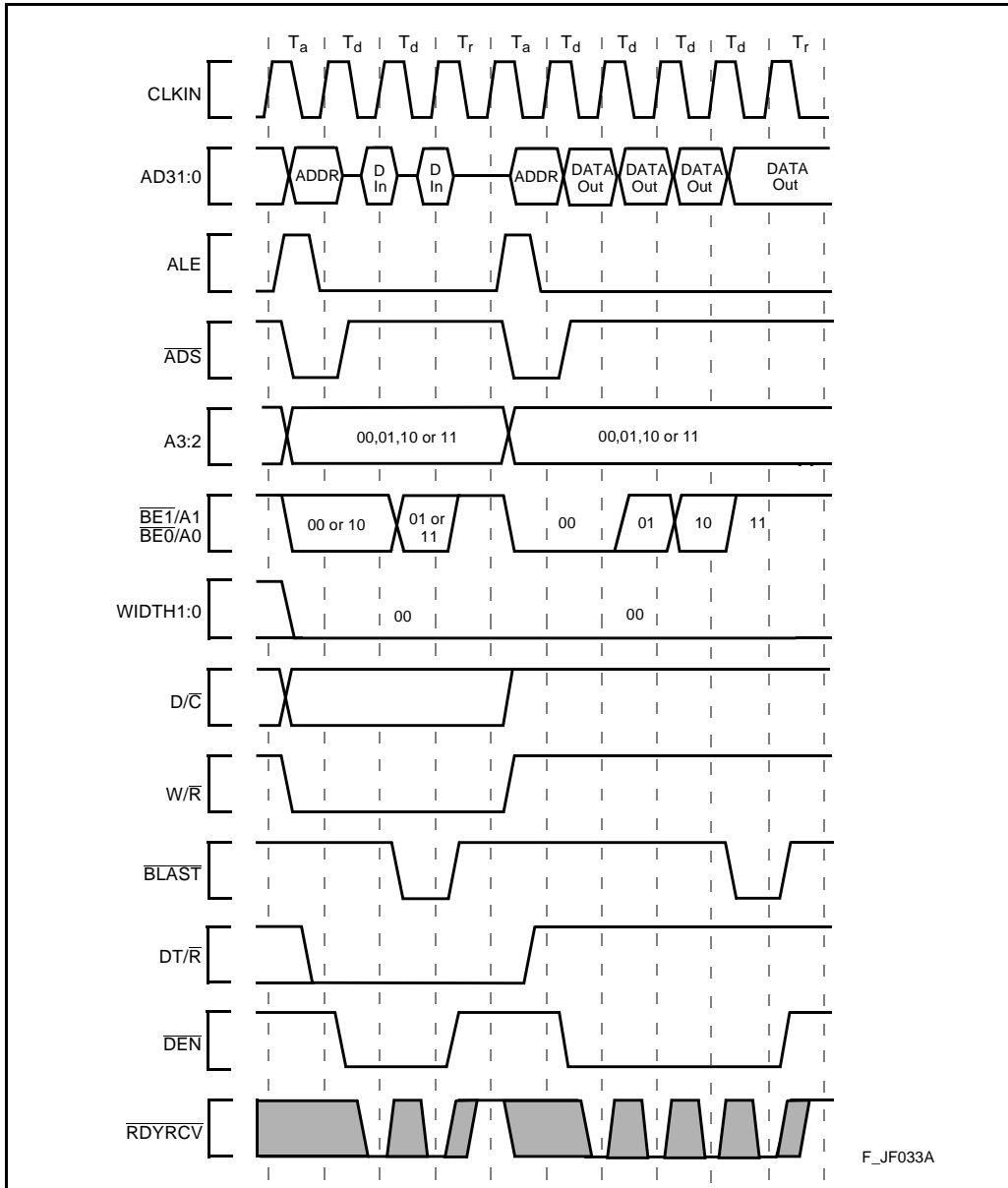


Figure 27. Burst Read and Write Transactions Without Wait States, 8-Bit Bus

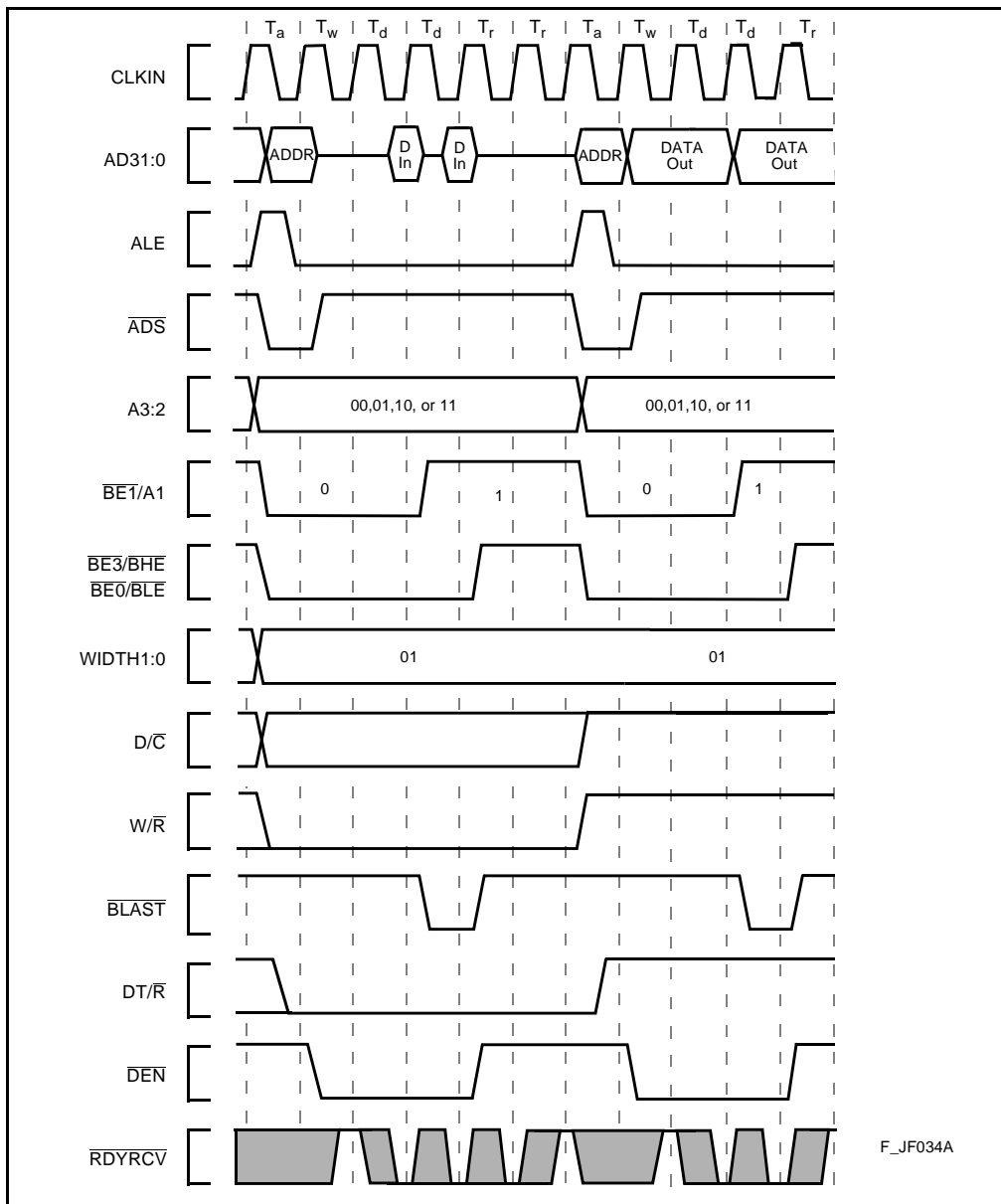


Figure 28. Burst Read and Write Transactions With 1, 0 Wait States and Extra T_r State on Read, 16-Bit Bus

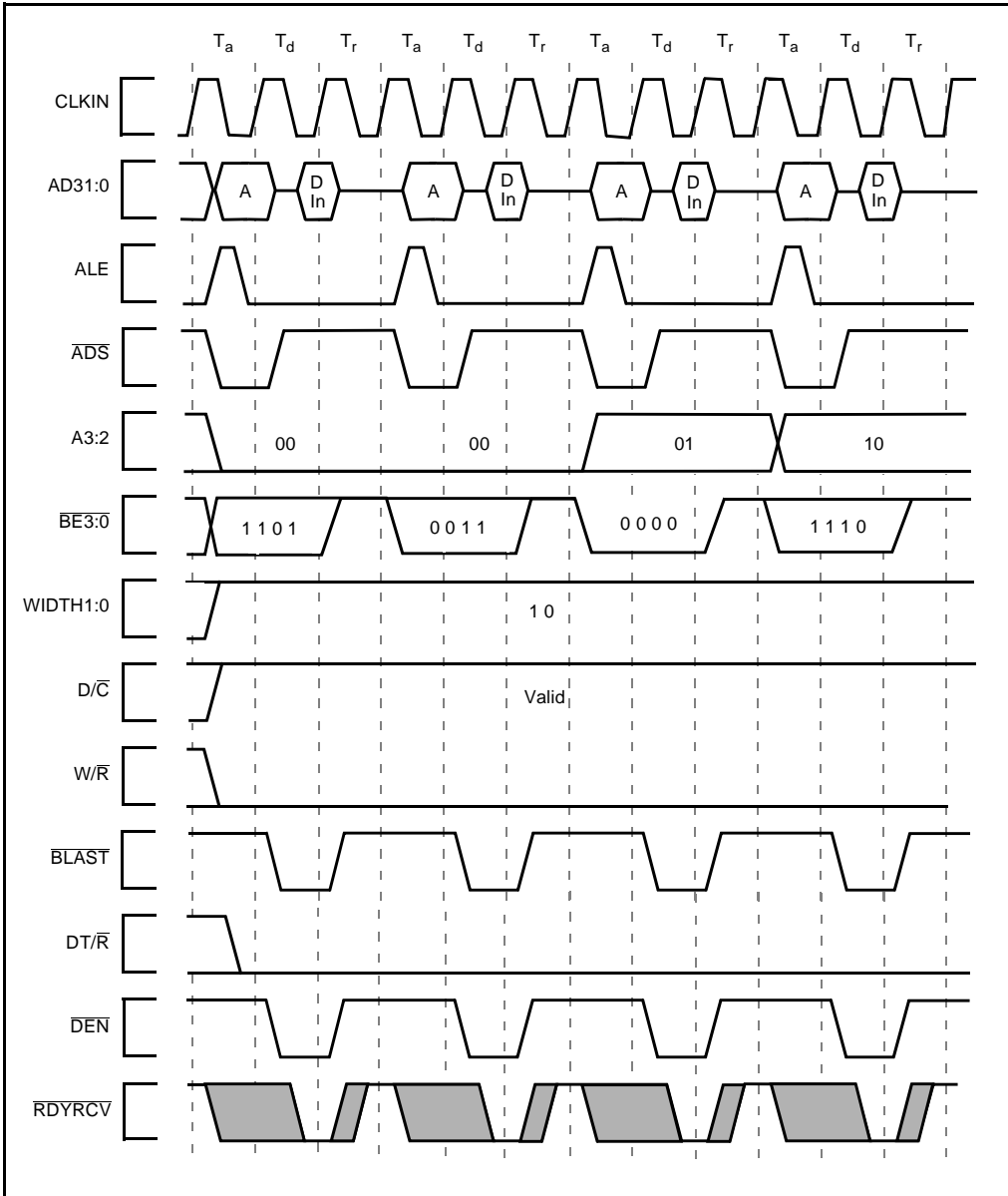


Figure 29. Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit Bus, Little Endian

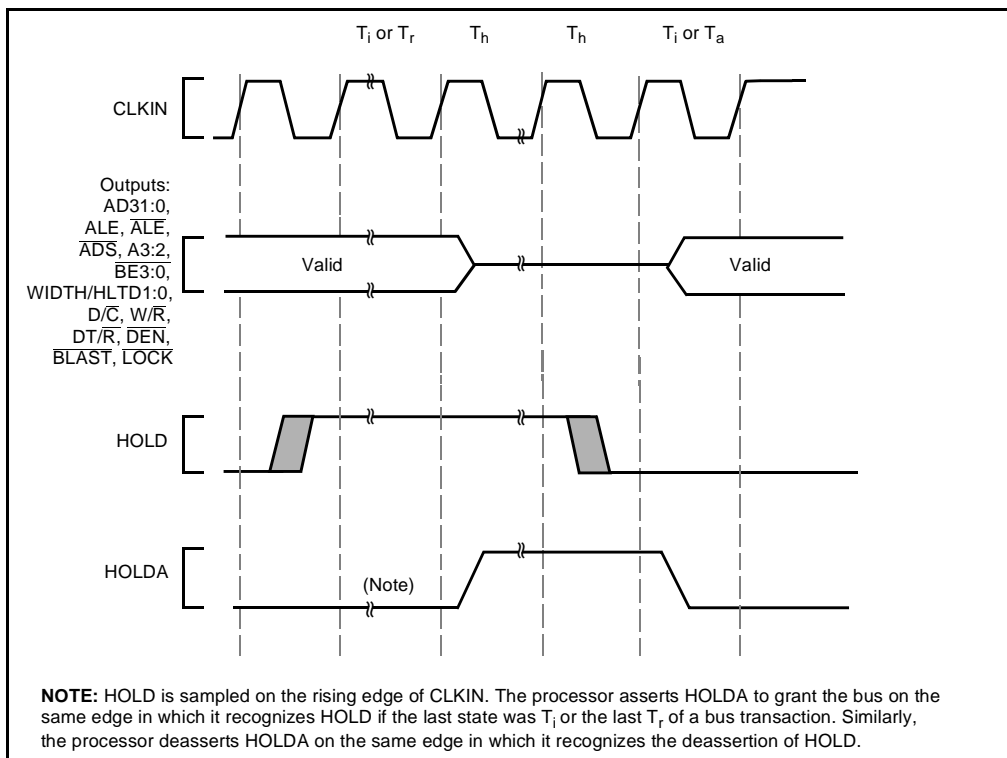


Figure 30. HOLD/HOLDA Waveform For Bus Arbitration

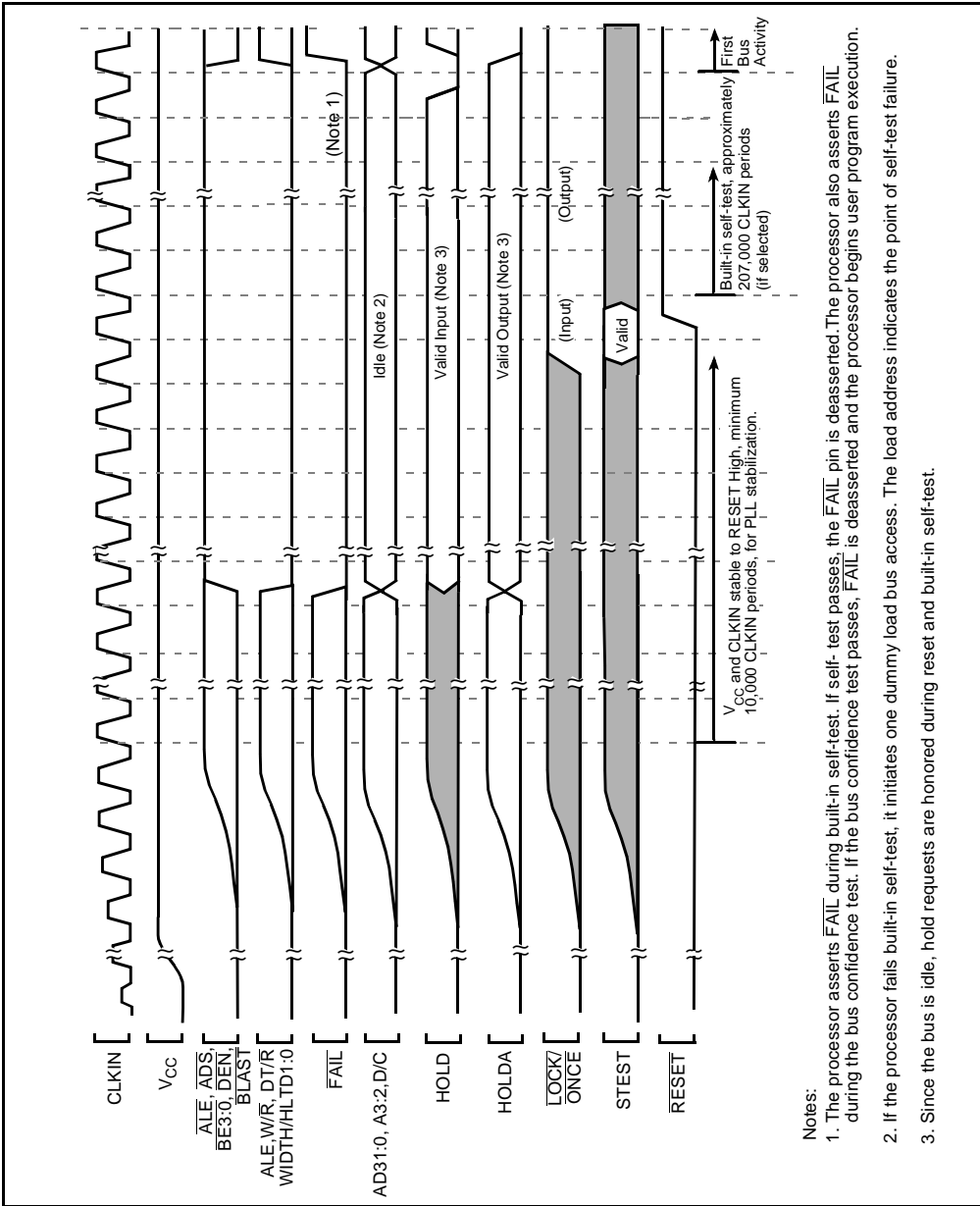


Figure 31. Cold Reset Waveform

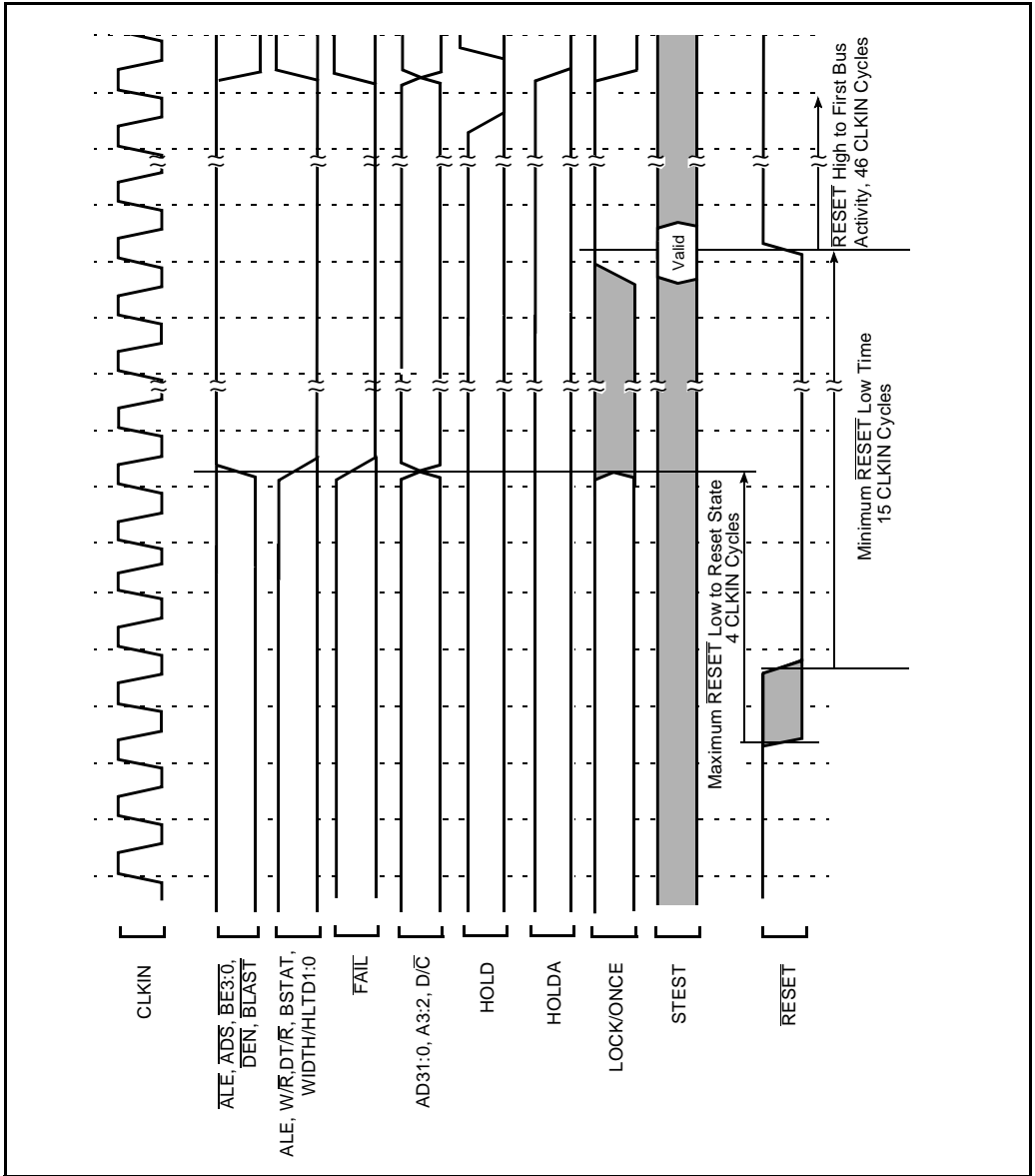


Figure 32. Warm Reset Waveform

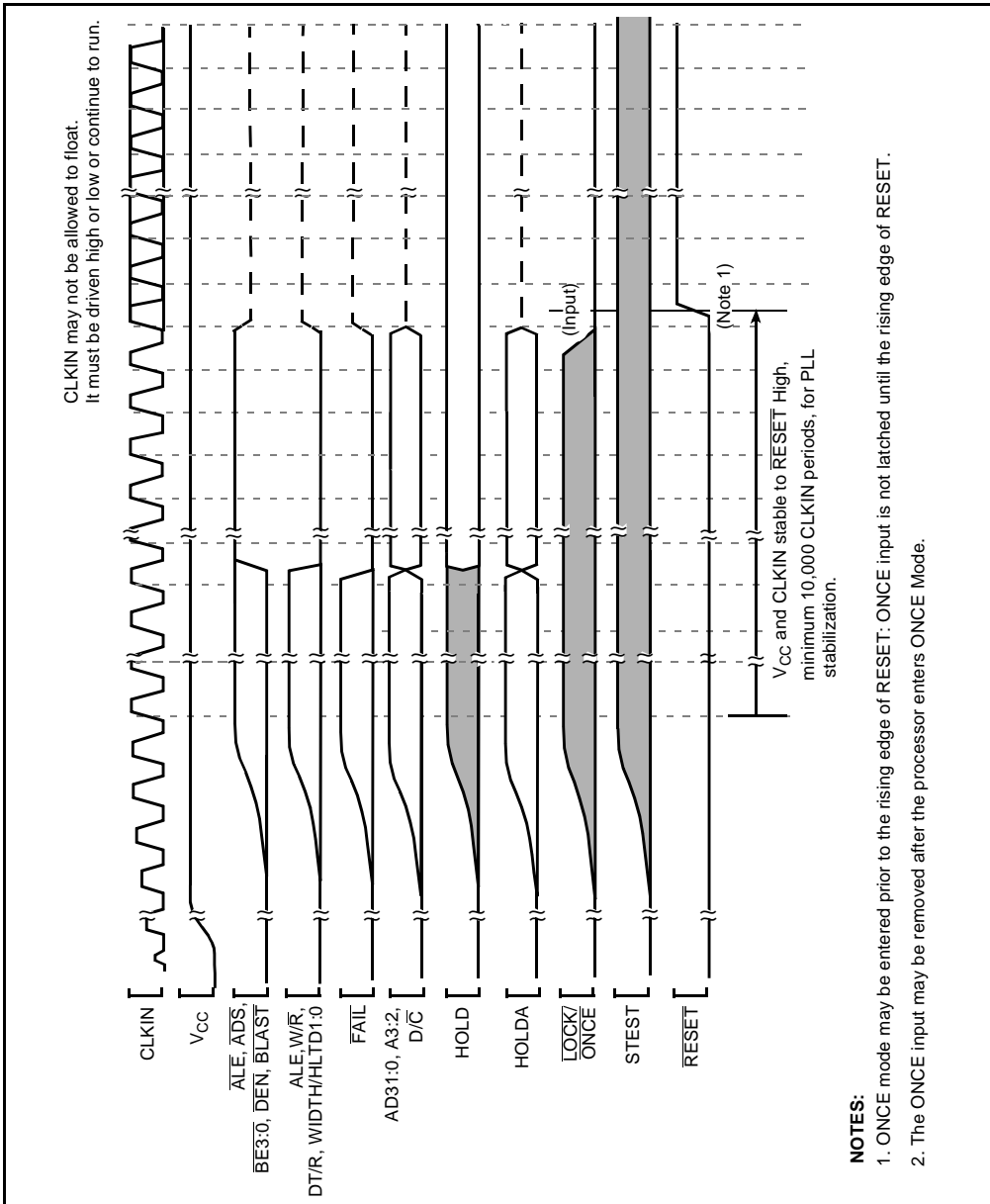


Figure 33. Entering the ONCE State

Table 18. Natural Boundaries for Load and Store Accesses

Data Width	Natural Boundary (Bytes)
Byte	1
Short Word	2
Word	4
Double Word	8
Triple Word	16
Quad Word	16

Table 19. Summary of Byte Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• byte access	• byte access	• byte access

Table 20. Summary of Short Word Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• burst of 2 bytes	• short-word access	• short-word access
+1	• 2 byte accesses	• 2 byte accesses	• 2 byte accesses

Table 21. Summary of n -Word Load and Store Accesses ($n = 1, 2, 3, 4$)

Address Offset from Natural Boundary in Bytes	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned) ($n = 1, 2, 3, 4$)	<ul style="list-style-type: none"> n burst(s) of 4 bytes 	<ul style="list-style-type: none"> case $n=1$: burst of 2 short words case $n=2$: burst of 4 short words case $n=3$: burst of 4 short words burst of 2 short words case $n=4$: 2 bursts of 4 short words 	<ul style="list-style-type: none"> burst of n word(s)
+1 ($n = 1, 2, 3, 4$) +5 ($n = 2, 3, 4$) +9 ($n = 3, 4$) +13 ($n = 3, 4$)	<ul style="list-style-type: none"> byte access burst of 2 bytes $n-1$ burst(s) of 4 bytes byte access 	<ul style="list-style-type: none"> byte access short-word access $n-1$ burst(s) of 2 short words byte access 	<ul style="list-style-type: none"> byte access short-word access $n-1$ word access(es) byte access
+2 ($n = 1, 2, 3, 4$) +6 ($n = 2, 3, 4$) +10 ($n = 3, 4$) +14 ($n = 3, 4$)	<ul style="list-style-type: none"> burst of 2 bytes $n-1$ burst(s) of 4 bytes burst of 2 bytes 	<ul style="list-style-type: none"> short-word access $n-1$ burst(s) of 2 short words short-word access 	<ul style="list-style-type: none"> short-word access $n-1$ word access(es) short-word access
+3 ($n = 1, 2, 3, 4$) +7 ($n = 2, 3, 4$) +11 ($n = 3, 4$) +15 ($n = 3, 4$)	<ul style="list-style-type: none"> byte access $n-1$ burst(s) of 4 bytes burst of 2 bytes byte access 	<ul style="list-style-type: none"> byte access $n-1$ burst(s) of 2 short words short-word access byte access 	<ul style="list-style-type: none"> byte access $n-1$ word access(es) short-word access byte access
+4 ($n = 2, 3, 4$) +8 ($n = 3, 4$) +12 ($n = 3, 4$)	<ul style="list-style-type: none"> n burst(s) of 4 bytes 	<ul style="list-style-type: none"> n burst(s) of 2 short words 	<ul style="list-style-type: none"> n word access(es)

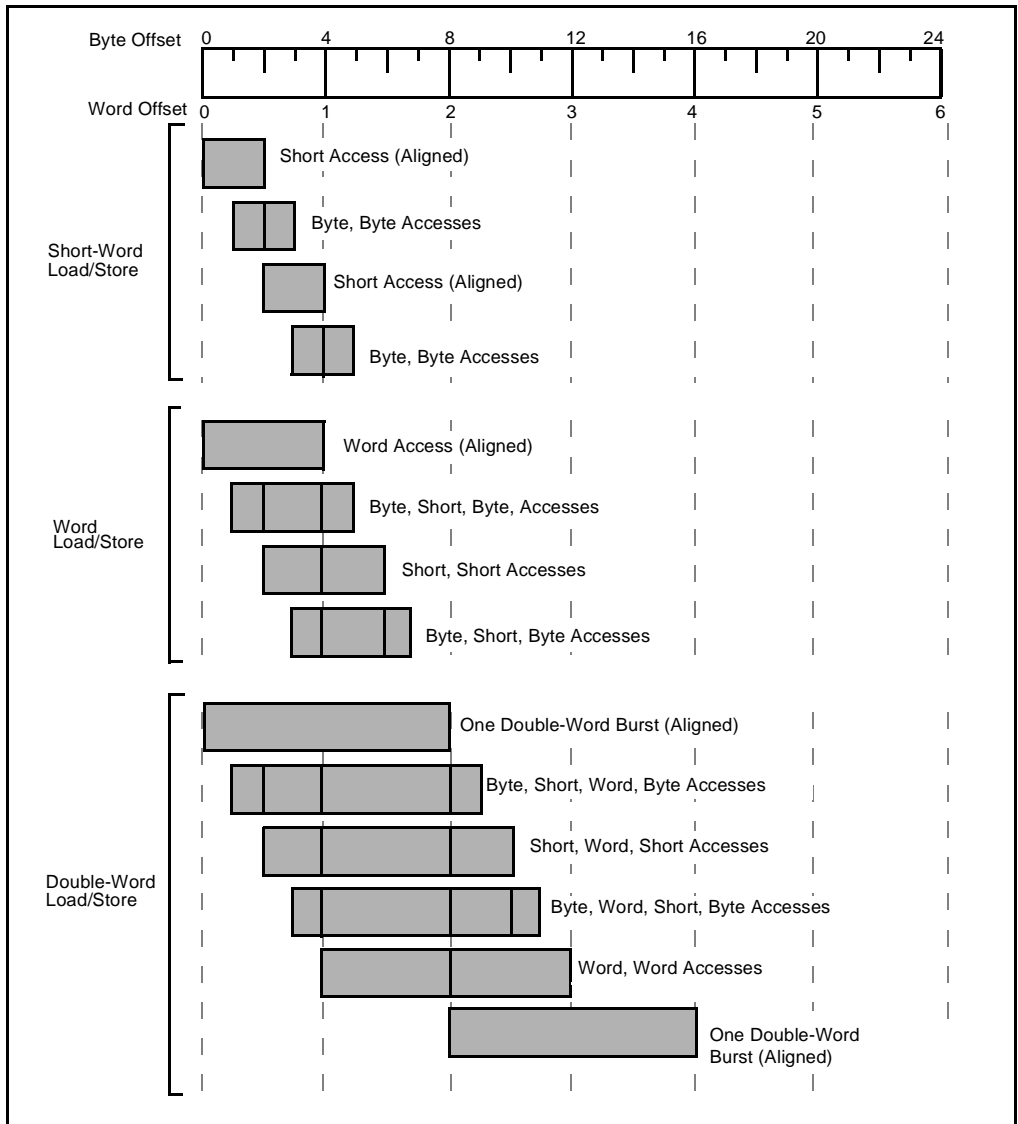


Figure 34. Summary of Aligned and Unaligned Accesses (32-Bit Bus)

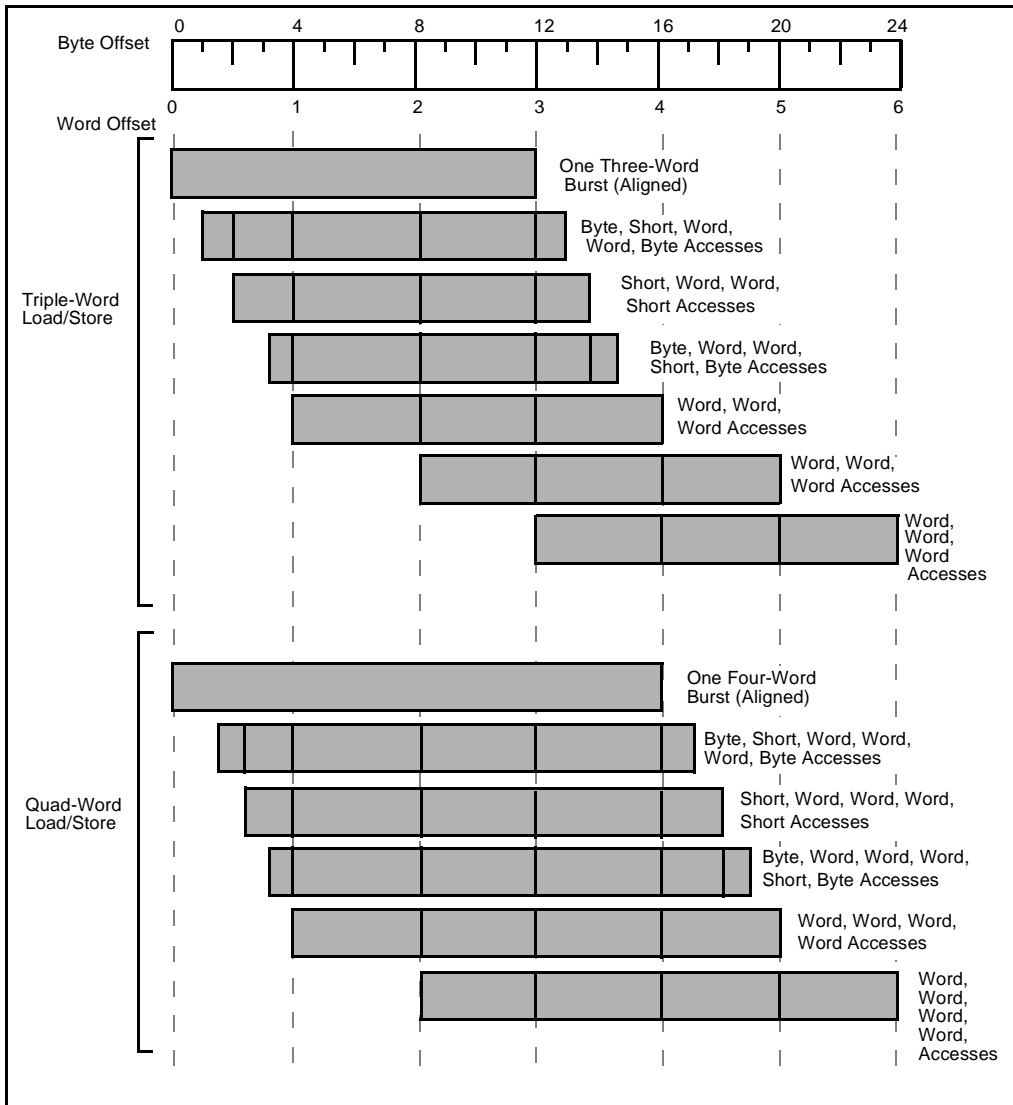


Figure 35. Summary of Aligned and Unaligned Accesses (32-Bit Bus) (Continued)

6.0 DEVICE IDENTIFICATION

80960JD processors may be identified electrically, according to device type and stepping (see Figure 36, and Table 22 through Table 25). Table 22 identifies the device ID for all 3.3 V and 5 V, 80960JD processors. Figure 36, and Table 23 through Table 25 identify all 3.3 V, 5 V-tolerant, 80960JD processors. The device ID for the C0 stepping is enhanced to differentiate between 3.3 V and 5 V supply voltages, and between non-clock-doubled and clock-doubled cores when stepping from the A2 stepping to the C0 stepping. The 32-bit identifier is accessible in three ways:

- Upon reset, the identifier is placed into the g0 register.
- The identifier may be accessed from supervisor mode at any time by reading the DEVICE ID register at address FF008710H.
- The IEEE Standard 1149.1 Test Access Port may select the DEVICE ID register through the IDCODE instruction.
- The device and stepping letter is also printed on the top side of the product package.

Table 22. 80960JD Die and Stepping Reference

Device and Stepping	Version Number	Part Number	Manufacturer	X	Complete ID (Hex)
80960JD A, A2	0000	1000 1000 0010 0000	0000 0001 001	1	08820013
80960JD C0	0011	0000 1000 0011 0000	0000 0001 001	1	30830013

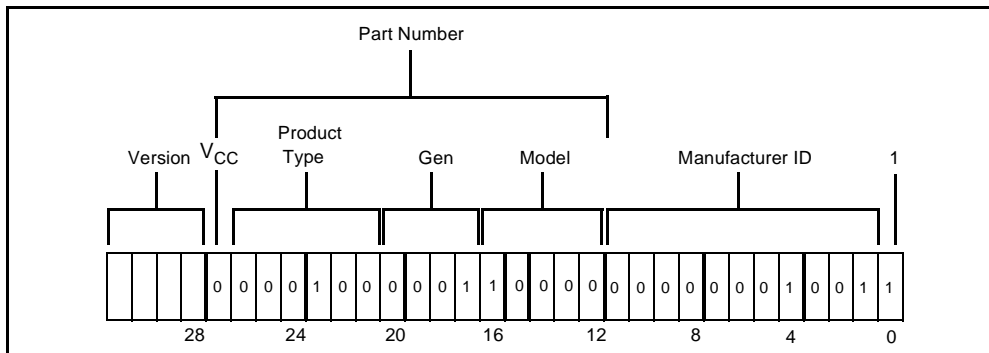


Figure 36. 80960JD Device Identification Register

Table 23. Fields of 80960JD Device ID

Field	Value	Definition
Version	See Table 25	Indicates major stepping changes.
V _{CC}	0 = 3.3 V device 1 = 5V device	Indicates that a device is 3.3 V or 5.0 V.
Product Type	00 0100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0001 = J-series	Indicates the generation (or series) of product.
Model	D000C D = Clock Doubled (0) Not Clock-Doubled (1) Clock Doubled C = Cache Size (0) 4K I-cache, 2K D-cache (1) 2K I-cache, 1K D-cache	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

Table 24. 80960JD Device ID Model Types

Device	Version	V _{CC}	Product	Gen.	Model	Manufacturer ID	'1'
80960JD A, A2	See	1	000100	0001	00000	00000001001	1
80960JD C0	Table 25	0	000100	0001	10000	00000001001	1

Table 25. Device ID Version Numbers for Different Steppings

Stepping	Version
A0	0000
A2	0000
C0	0011

NOTE: This data sheet applies to the 80960JD C0 stepping.

7.0 REVISION HISTORY

This is the first revision of the 3.3 V device.